



LET A HUNDRED FLOWERS BLOSSOM

Local Competition and the Rise of Chinese
Semiconductor Capacity

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Research Institute for Democracy, Society and Emerging Technology (DSET)

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Executive Summary

Rising Chinese semiconductor manufacturing capacity across process nodes and products in terms of global shares could be attributed to :

- Central government corporate and VAT tax cuts since 2000 and equity guidance funds represented by the Big Fund since 2014
- Local government discretionary subsidies that target IC design and manufacturing input costs or reward sales or R&D output, local venture capital and equity guidance funds, and infrastructure support via establishing industrial parks and clusters
- In particular, local government pioneered the government venture capital model that became the salient instrument to support semiconductor manufacturing in China. Local governments supported national champions such as SMIC, CXMT, and Huahong early on via this method.

In particular, Chinese “overcapacity” and lower prices in mature node semiconductors are consequences of :

- Intense subsidy competition between local governments to maximize local semiconductor output and cultivate local champions across various niche subsectors.
- As the entire electronics supply chain is supported with total output being the target, governments do not prioritize manufacturing profits, resulting in rising capacity and lower wafer prices. This reduces input costs of downstream design & product firms and generates incentives to order from local manufacturers, facilitating dynamic manufacturing cost reduction through learning by doing.

To address Chinese overcapacity concerns, unilateral tariff regimes are ineffective to protect domestic producers as :

- Chinese manufacturers are competing with other countries' mature chipmakers for customers within China and other countries, as Chinese domestic self-sufficiency remains low even in mature node semiconductors;
- Imported Chinese chips are likely to be embedded in electronic components that get shipped across multiple borders, making it impossible for customs to determine its origin in a reasonable component tariff regime, especially when importers have strong incentives to mark down the percentage of value produced in China

A joint sectoral agreement between the US, Europe, and likeminded East Asian countries to determine joint tariffs and outbound investment restrictions, establish within-bloc free trade across the supply chain, and coordinate on capacity and specialized process R&D is instead recommended to :

- Consolidate production and integrate the expertise of American, European, Taiwanese, and Korean foundries to not fall into spiraling price wars with each other and Chinese producers
- Ensure sufficient within-bloc demand for allied country producers' products

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Introduction

The global semiconductor landscape has undergone a dramatic transformation since China made achieving domestic self-sufficiency in semiconductor production a national priority in Made in China 2025. On the technological frontier, Chinese firms continue to make surprising advances in [memory](#)¹, [compound semiconductor](#)², and even [logic chip manufacturing](#)³ despite increasingly stringent US export controls. On mature semiconductors of processes at 28 nanometers and above, Chinese firms have been ramping up capacity in a dramatic fashion, now taking up a significant portion of global capacity and [threatening the profitability of western and other East Asian competitors](#)⁴ with low prices. Commentators often explain the rise of Chinese semiconductors as an outcome of Chinese industrial policy such as the [National Integrated Circuit Industry Investment Fund](#)⁵ (the “Big Fund”). But a better question to ask is: what industrial policy propelled the rise of Chinese semiconductors despite sanctions and trade wars?

This piece documents that Chinese semiconductor industrial policy differs from that of the Western world and other East Asian countries fundamentally in two respects: (I) local governments at the provincial, municipal and sub-municipal levels have significant discretion and resources to direct support to local firms. Local subsidy programs are often made with explicit intention to compete with

other localities in the same subsector of the semiconductor supply chain. For example, [Shenzhen](#)⁶, long seen as the “Silicon Valley” of China hosting dominant design and downstream product firms like Huawei, Tencent, DJI, and BYD, is now committed to bolstering local semiconductor fabrication capabilities. It is explicitly targeting to become the “third pole” of China’s semiconductor manufacturing, with reference to the other two manufacturing strongholds: Beijing and Shanghai. (II) the scope of government support covers the entire supply chain from upstream semiconductor design and software, materials and equipment, to wafer fabrication and downstream packaging & testing, printed circuit boards, and assemblies. Final electronic products that use semiconductors are also heavily subsidized, for example, AI servers, consumer electronics, drones, and EVs. This is rare globally as typically countries target segments of the semiconductor value chain where they consider themselves less competitive: the US CHIPS Act focuses on semiconductor manufacturing with little emphasis on design, while Taiwan’s Chip-based Industrial Innovation Program targets advancements in design and advanced packaging.

Hence, Chinese semiconductor industrial policy is a combination of central government directives, tax breaks, and equity investments with specific local government programs of cost & performance-based subsidies and equity

injections targeting the entire semiconductor value chain. Political economy considerations, a consequence of China's "tournament model" in which local officials are evaluated on local economic performance, result in a policy emphasis on creating domestic supply chains at the local level. Local governments subsidize all priority sectors in a "beggar-thy-neighbor" fashion, with little regard to local comparative advantages in an essentially national market. Intense competition between local-government-supported champions in narrow subsectors of the industry generates static inefficiency as many nationally uncompetitive firms expand production with subsidized costs, depressing national and global prices. On the other hand, a benefit of such a holistic approach targeting the entire value chain is that buyers downstream enjoy cheaper inputs, which they obtain through competition between multiple suppliers across the nation as well as incentives from procuring locally. Subsidies to the upstream as a result would reduce the subsidies needed to support downstream applications, while downstream subsidies themselves also create demand for upstream inputs. Incentivizing downstream demand for domestic home production in turn justifies upstream manufacturers' capacity expansion, facilitating dynamic cost reductions through learning-by-doing.

The empirical part of the paper evaluates the effectiveness of decentralized industrial policy by asking whether the central and local governments have the ability to select productive and innovative firms *ex ante* or promote firms to be globally competitive *ex post*. Specifically, I study equity investments by the central and local governments to semiconductor firms through venture capital-

like vehicles such as the government guidance fund, the most salient instrument through which the Chinese governments support the semiconductor industry⁷. Given that local governments' policy documents ubiquitously set maximizing regional output or sales as the policy objective, governments should prioritize investing in productive firms, defined as firms that could generate higher output and capacity given capital stock. I formally test this prediction by estimating plants' capacity productivity, a measure of plants' idiosyncratic capability to convert capital expenditures to production capacity, given data on plants' capacity, equipment/construction investment costs, and process technology.

Initial results suggest that although the central government does not seem to allocate equity investments to more productive firms nationally *ex ante* or make them more productive *ex post*, provincial governments' portfolios are mostly concentrated on more productive firms *within their province*. Provincial champions may not be the most productive national champions, thus nationally substantial government equity investments seem to have been directed to unproductive firms.

Hence there is misallocation of government equity capital *statically* at the national level, but provincial equity investments seem to be well directed for local governments' purposes. Furthermore, locally-invested firms seem to have improved their productivity, benchmarked with their national firms, over a longer time horizon, suggesting that decentralized industrial policy in China may yield *dynamic benefits*. Yet there is also little evidence government champions, whether central or local, innovated

more to produce more advanced processes than other domestic firms. This is consistent with the narrative that Chinese political economy incentives are skewed towards promoting capital investments that stimulate short-run GDP rather than risky innovation that yield potentially high but uncertain long-term benefits⁸.

The paper is organized as follows: Section 1 summarizes the primary policy tools through which the Chinese central government and local governments support semiconductors and provides a broad overview of the semiconductor value chain in China. Section 2 describes the data and documents how decentralized industrial policy and local governments' policy emphasis on maximizing local output lead to capacity buildup and reduced prices. Section 3 concludes.

Chinese Semiconductor Industrial Policy

The Semiconductor Value Chain in China

Semiconductors could first be categorized into discrete devices, a single diode or transistor typically used to manage power and signal transmission in electronics and automotive, and more complicated integrated circuits (ICs) that have hundreds to billions of transistors on a single chip. ICs serve different functions that could be broadly classified into the following categories: logic chips such as CPUs, GPUs, and ASICs (application-specific integrated circuits) process digital data (0s and 1s) to perform arithmetic calculations and generate digital output. Memory chips including DRAM and NAND Flash store digital data. Analog ICs process continuous (analog) signals widely used in power management, sensing, wireless communications, and audio/signal processing applications. Technological prowess of a manufacturing process could be represented by its process node, typically measured in microns or nanometers (nm, 0.001 micron). A smaller number indicates a more advanced process. The number in the past referred to the minimum gate length between transistors of an integrated circuit. The advent of the 28nm process saw transistor architecture moving from the planar MOSFET transistor to a 3D FinFET transistor, making new nanometer nodes more of a marketing term that no longer refers to any physical properties of the IC. Still, for each major node improvement (14 to 10 to 7 nm for example), transistor density, which affects computational performance per unit of energy consumption, is expected to improve by 20~30% .

The semiconductor industry supply chain could be broadly classified into three segments:

design, fabrication (frontend manufacturing), and packaging & testing (backend manufacturing). Furthermore, each segment in return requires upstream input. IC designers need to procure electronic design softwares (EDAs) and intellectual property blocks (IPs) to design intricate and dense ICs electronically via code. IC fabrication firms use a variety of equipment and chemicals for each step of their manufacturing process to inscribe digital circuitry onto physical silicon or compound semiconductor wafers. The wafers produced by frontend manufacturers, measured in size by its diameter ranging from 4 to 12 inch, are in turn cut into dies, packaged into microchips with interconnects, and tested by the facilities with relevant packaging & testing equipment. Traditionally in the integrated device manufacturer (IDM) model, a firm designs, manufactures, packages, and distributes its product. Major memory producers such as Samsung, SK Hynix, and Micron, analog/discrete devices manufacturers such as Texas Instruments, as well as some microprocessor firms like Intel pursue this model. The creation of the "foundry model" by Taiwan Semiconductor Manufacturing Company (TSMC) revolutionized the industry. "With "pure play foundries" laser-focused on manufacturing products designed by other firms, IC design firms can now focus on designing and marketing products while avoiding the increasingly prohibitive upfront capital investment that IC fabrication requires. As a result, countless IC design firms globally could enter the market by outsourcing to foundries like TSMC.

Closing on the Frontier: Design, Manufacturing & Packagin

The success of the foundry model accelerated the development of China's semiconductor industry. Rapid growth of China's downstream electronics market and access to leading Taiwanese foundries fueled the entry of numerous IC design firms that grew to be competitive vis-a-vis global firms. By far the most successful IC designer is Huawei's HiSilicon, known for developing smartphone chipsets and more recently server CPUs and GPUs for artificial intelligence applications. Other notable design firms include UNISOC (Spreadtrum) and ZTE Sanechips for smartphone chips, Will Semiconductor and Goodix for image and touchscreen sensors, Loongson and Hygon for microprocessors, Bitmain for mining ASICs, and Cambricon/Biren/Moore Threads for AI accelerators.

On the fabrication side, Semiconductor Manufacturing International Corporation (SMIC) is the dominant domestic Chinese player. Founded by former TSMC executive Richard Chang, SMIC epitomizes the exodus of Taiwanese investment, technology, and talent that created the impetus for the growth of China's domestic semiconductor industry⁹. SMIC became increasingly important in advancing Chinese homegrown process technologies as stringent US export controls have denied many Chinese firms from accessing TSMC's leading nodes. Despite US Entity List controls that prevented acquisitions of Dutch firm ASML's advanced EUV (extreme ultraviolet) lithography machines, SMIC continued to advance its process node using older

generation DUV (deep ultraviolet) machines. It sent [shockwaves](#)¹⁰ in Washington when it debuted a 7nm-equivalent process found in Huawei's smartphones and GPUs in 2023. On the less advanced nodes, SMIC and other Chinese foundries like Huahong/Shanghai Huali, Hefei Nexchip, Qingdao SiEn, and IDMs including Silan, CR Micro, and Sanan have been ramping up production capacity and yield to challenge foreign competitors. Another notable development is the emergence of multiple manufacturing firms across DRAM, logic, and sensing/radio-frequency IC in Shenzhen, funded completely by Shenzhen's Major Industry Investment Group. These firms were thought to be affiliated with [Huawei](#)¹¹, suggesting Huawei is moving from a pure design and product company to [a vertically integrated national hardware champion](#)¹².

The rise of Chinese production capacity and technology capabilities in the commodified memory and compound semiconductor sectors have been pressuring global prices and industrial profits. In DRAM (RAM memory), Hefei's CXMT [has taken a significant market share](#)¹³ in the legacy DDR4 market and is now entering the frontier DDR5 and high-bandwidth memory (HBM) market critical for AI applications. Wuhan's YMTC via its proprietary Xtacking architecture has reached the global technological frontier in NAND Flash (hard disk drive) by introducing [a 294-layer 3D NAND chip](#)¹⁴. These two firms are now threatening to break up the memory triopoly of Samsung, SK Hynix, and Micron despite US sanctions. In compound semiconductors such as silicon carbide (SiC) and gallium nitride (GaN), Chinese firms are now expected [to take up more than](#)

[50% of global capacity](#)¹⁵ driven primarily by Chinese dominance in downstream applications like EVs, 5G/6G telecommunications, and solar panels that require high-power and high-frequency-resilient compound materials. Notable champions include SICC and TanKeBlue for SiC wafers, InnoScience and Suzhou Nanowin for GaN wafers, and Sanan and Silan for compound semiconductor manufacturing. Driven by the desire to continue accessing China's growing auto market, European power and analog IDMs such as STMicro and NXP are building capacity and [forming joint ventures](#)¹⁶ in China in close cooperation with local compound semiconductor manufacturers and wafer suppliers.

Chinese firms have long occupied significant market shares in the traditionally lower value-add packaging & testing space, represented by companies like Jiangsu Changjiang Electronics Technology (JCET), Tianshui Huatian, and Tongfu Microelectronics. As Moore's Law advances to its limits, advanced packaging techniques that improve interconnectivity between chip components have become increasingly important relative to traditional die shrinkage in frontend manufacturing. Chinese firms have also been [accelerating investments in advanced packaging](#)¹⁷ capacity including wafer-level and panel-level packaging, though their technology sophistication appears to remain a generation behind that of Taiwanese leaders like TSMC and SPIL. With recent US sanctions now [prohibiting IC designers of chips below 16-nm](#)¹⁸ to access Chinese packaging firms, domestic advanced packaging has now become another less noticeable yet critical priority for China to fully localize high-performance computing IC

production. Apart from CXMT who does 2.5D to 3D packaging for in-house HBM production, JCET via its subsidiary JCET Shaoxing is [aggressively expanding](#)¹⁹ advanced packaging capacity in a joint venture with the Big Fund and Zhejiang Industrial Fund, with technology transferred from its Korean subsidiary.

Figure 1: The Chinese Semiconductor/Electronics Supply Chain (Adapted from a presentation of Randy Abrams from Credit Suisse²⁰)

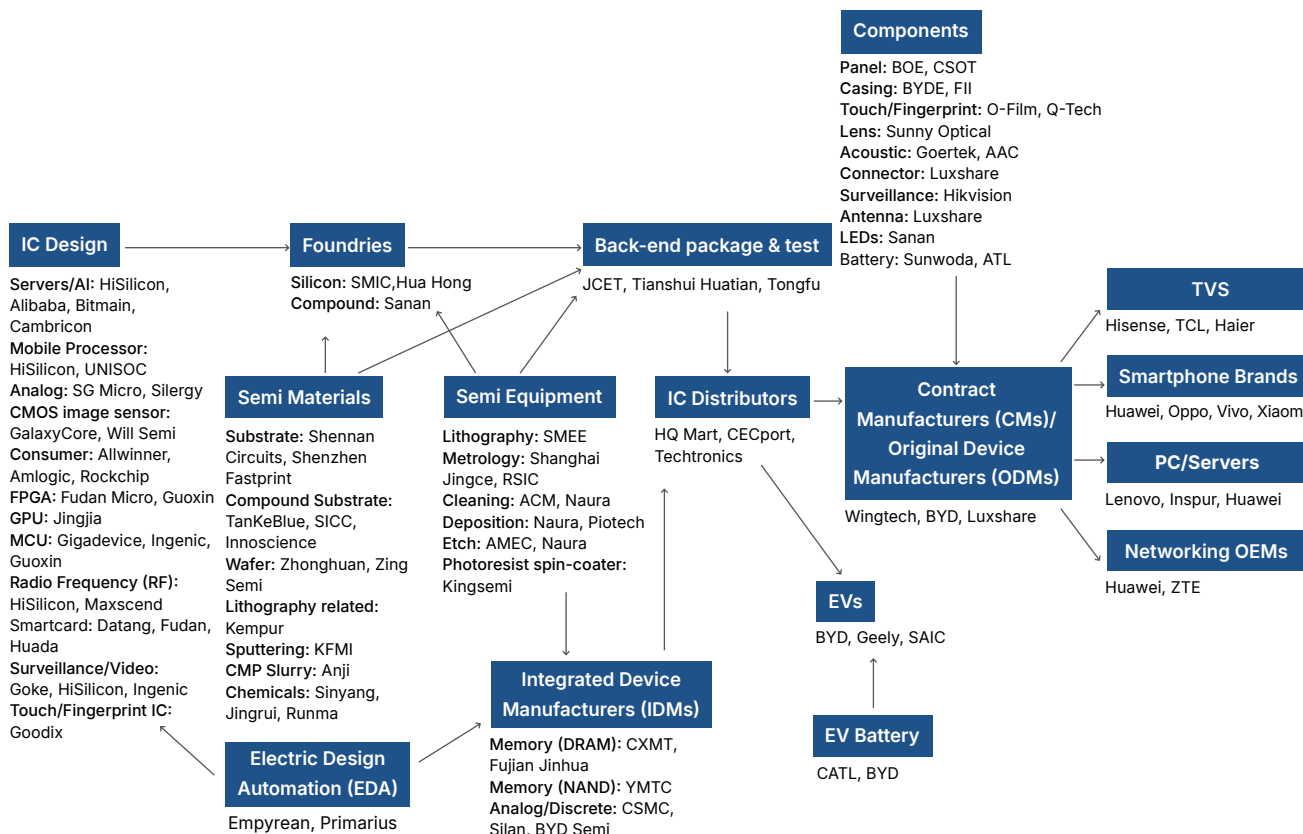
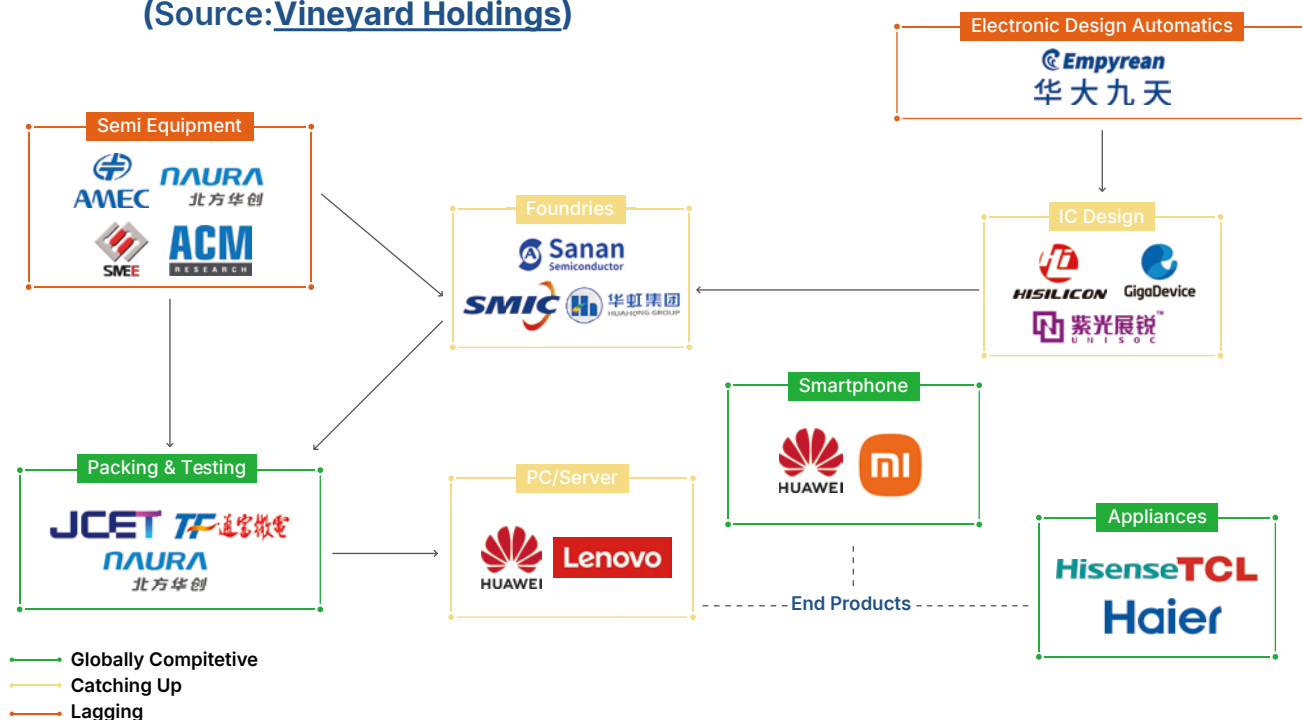


Figure 2: The Semiconductor Supply Chain and Key Companies in China (Source: Vineyard Holdings)



Chokepoints: EDA, manufacturing equipment, photoresist materials

Though Chinese firms have made significant progress in semiconductor design and manufacturing, the critical inputs of these sectors, ranging from software, equipment, to materials, still rely very much on foreign firms. One critical input for IC design firms is EDA (Electronic Design Automation) tools, essential for IC designers to design, simulate, and verify functionalities of their circuit blueprints via code. The EDA market is dominated by three US-based firms: Cadence, Synopsys, and Siemens EDA (ex Mentor Graphics), [occupying over 80% of the market share in China](#)²¹. Domestic alternatives offered by state champions like Empyrean and Primarius could only cover parts of the design flow for processes below 28 nanometers. Huawei has developed its own in-house EDA solutions [for 14nm designs](#)²². US sanctions have prevented chip designers on the Entity List, such as Huawei HiSilicon, from accessing US EDA tools. All Chinese firms were also barred from using EDA tools [supporting GAAFET transistor architecture](#)²³ essential for sub-3nm designs. Hence, Chinese firms are unlikely to design and mass-produce any chip below 5nm technology without significant improvement in domestic EDA capabilities.

Another sector in which Chinese firms are generations behind the global frontier is semiconductor manufacturing equipment. Each specific manufacturing process, from deposition, photoresist coating, lithography, etching, ion implantation, to cleaning, requires different tools that have been dominated by a

few global firms. Most famously, lithography machines including DUV and EUV tools essential for sub-90nm processes are monopolized by Dutch firm ASML. Chinese firm [Shanghai Micro Electronics Equipment \(SMEE\)](#)²⁴ in 2024 and [Shenzhen SiCarrier](#)²⁵ in 2025 claimed to have developed lithography machines (scanners) suitable for 28nm processes, though there is little evidence that such machines are in commercial production. [SMEE](#)²⁶ makes legacy I-Line, KrF (krypton-fluoride), and ArF (argon-fluoride) scanners capable of making 280-90nm, and was thought to have developed technologies for 65nm processes according to an announcement by [China's Ministry of Industry and Information Technology \(MIIT\)](#)²⁷ in 2024. Chinese firms still rely on imported ArF/ArFi DUVs for both mature node and advanced node semiconductors. Without access to ASML's advanced EUVs, SMIC/Huawei have to rely on costly [double or quadruple patterning processes with DUVs](#)²⁸ to produce sub-10nm process chips, which leads to substantial yield loss in production.

Other processes ranging from etching, ion implantation, deposition, to chemical mechanical planarization (CMP) are dominated by American and Japanese suppliers Applied Materials, Lam Research, and Tokyo Electron. Pushed by Western export controls and government self-sufficiency efforts, Chinese equipment manufacturers like NAURA, AMEC, and ACM Research have seen increasing sales and market shares in these segments. [A 2025 TrendForce report](#)²⁹ suggests that Chinese firms have achieved significant self-sufficiency in photoresist stripping, cleaning, etching, and thermal processing tools, taking up over 30% of

the domestic market share with over 50% for mature processes. For CMP and physical vapor deposition (PVD), Chinese firms have 20% market share for mature node processes. In chemical vapor deposition/atomic layer deposition (CVD/ALD), ion implantation, metrology (testing), and coating & developing, Chinese domestic sales share amounts to about 10% for mature processes.

Photoresists, the materials that are exposed to light to create circuit patterns in the lithography process, are a less well-known area in which Chinese firms depend on foreign suppliers from Japan (JSR, TOK, Shin-etsu, Sumitomo, & Fujifilm) and the United States (Dupont). [Chinese market share³⁰](#) for photoresists in the legacy i-line lithography amounted to less than 20%, <5% for KrF DUV lithography, and <1% for the more advanced ArF DUV lithography. As photoresist materials could not be stored for more than 6 months, potential future export controls of this item could be fatal to the Chinese industry. Significant R&D and venture capital investments were made to support [selected firms³¹](#) such as Beijing Kempur and Nata Opto “Special project on very large scale integrated circuit manufacturing equipment” Theme of the “National Science and Technology Project”. Beijing Kempur, acquired by Red Avenue Materials, first achieved mass-production of KrF photoresists in 2017. Numerous firms including Nata, Kempur, Hubei Dinglong, and Xuzhou Bokang [have now successfully developed³²](#) ArF photoresists for small volume production.

Chinese and Global Semiconductor Equipment Manufactures

Table 1: Semiconductor Equipment Market shares in China (Source: TrendForce³³)

Equipment Category	Self-Sufficiency Rate	Chinese Company	Global Company
Photoresist Stripping	75%-90% (low-end) <30% (high-end)	BEST, NAURA, ACM, ZheJiang YuQian, JET PLASMA	Hitachi High-Technologies, Lam Research
Cleaning	50-60%	ACM, NAURA, PNC, Kingsemi, BEST	SCREEN, Tokyo Electron Limited, Lam Research
Etching	50%-60% (mature process) <15% (advanced process)	AMEC, NAURA, Joysingtech, BEST, Piotech, ACM, Kingsemi	Applied Materials, Lam Research, Tokyo Electron Limited
Thermal Processing	30%-40%	NAURA, JSG, AMEC, Piotech, Joysingtech	ASM International, Applied Materials, Lam Research, Tokyo Electron Limited
PVD	15%-20% (mature process) 10% (advanced process)	NAURA, SC, Joysingtech, CETC, HF-Kejing	ASM International, Applied Materials, Lam Research, Tokyo Electron Limited
CVD/ALD	5%-10%	NAURA, JSG, AMEC, ACM, Piotech, Joysingtech	ASM International, Applied Materials, Lam Research, Tokyo Electron Limited
CMP	15%-25% (mature process) <10% (advanced process)	ACM, Hwatsing, CETC, Hubei Dinglong	DuPont, Thomas West Inc, JSR
Coating and Developing	10%-15% (mature process) <10% (advanced process)	ACM, Kingsemi, NAURA, AMEC, Beijing Huafeng & Control	Dow Chemical, JSR, TOK America
Ion Implantation	10%-20% (mature process) <5% (advanced process)	Kingstone, CETC, NAURA, AMEC	Applied Materials, Axcelis Technologies
Metrology	10%-15% (mature process) <5% (advanced process)	SMEE, Skyverse Technology, Jingce, Hwatsing, NAURA	KLA, Santec Holdings Corporation
Lithography Equipment	10%-15% (mature process) <0%-1% (advanced process)	SMEE, CETC, NAURA	ASML, Canon, Nikon

Central Government Policies: Tax Breaks, Guidelines, Equity Investments

The modern integrated circuits industry in China began with the “008” and “909” projects to create state-owned enterprises in semiconductor manufacturing, which became the predecessors of power semiconductor manufacturer CR Micro and China's 2nd largest foundry Huahong respectively. These SOEs were established to form joint ventures with foreign companies to exchange market access and state subsidies in return for foreign technologies. For example, Huahong partnered with Japanese manufacturer NEC to form HHNEC to build China's first commercial 200mm fab. These SOE³⁴-JVs did not have much success in advancing domestic frontier technologies or even achieving commercial viability, while instead non-SOEs such as SMIC showed promise. China's rapid economic ascent to become the world's electronics manufacturing hub, rising domestic consumer demand as well as the perceived failures of the 908 and 909 projects pushed the Chinese State Council to pivot away from central planning to market-based industrial policy. Instead of creating state-owned enterprises, the state now offers tax and other subsidy incentives designed to reduce input costs of any eligible firms, regardless of state ownership or even nationality.

In January 2000 the State Council announced *Several Policies to Encourage the Development of the Software Industry and IC Industry* (“Document No.18”) to cut the value added tax (VAT) from 17 percent to 3 percent for ICs fabricated or designed in China, regardless

of firm nationality, while also offering the famous 2+3 income tax break (liang mian san jian ban: two years tax exemption and three years of 50% reduction in tax) for IC design firms and manufacturers with <0.25 micron process and/or with investments over 8 billion RMB. Firms also would receive zero import duties on technology and IC capital equipment. The implementation of the policy was marred by the US government's complaints that these tax breaks violated WTO rules, which led to the rescinding of the VAT tax break in 2004 and long administration process of recognizing domestic design operations. A new round of tax incentives, [*“Several Policies to Further Encourage the Development of the Software Industry and the Integrated Circuit Industry”*](#)³⁵ (“Document No.4”), was announced in 2011, which extended the 2+3 tax cuts to manufacturers of line-width technologies <0.8 microns as well as new IC design and qualified software firms. In addition, > 15 years old firms with technologies <0.25 microns or with investments of over 8 billion RMB enjoyed five years of tax exemption and five years of halved corporate income tax. Still, many state-owned IC design and fabrication firms primarily lived off state procurement, most notably the “Golden Card Project” which designated state-owned firms such as Leadcore and CEC Huada to make IC cards with chips, such as ID, telephone or transportation cards. These procurement projects typically relied on simpler technology processes and did not give state-connected firms incentives to engage in technology upgrading.

The watershed moment of Chinese semiconductor industrial policy arrived in June 2014 when the central government promulgated

the “[National Integrated Circuit Industry Development Promotion Outline](#)”,³⁶ with the stated goal for Chinese production to attain 70% of domestic demand by 2025 (15% in 2014). It established a “National Integrated Circuit Industry Investment Fund” that raised around 138.7 billion RMB in its initial funding round (“Phase I”) in August 2014 from the Ministry of Finance, central SOEs like China Development Bank and China Tobacco, and local government funds and SOEs such as Beijing E-Town and Shanghai Guosheng Group. The fund is managed by Sino IC Capital and invested in minority stakes of both publicly-listed and private companies. “Phase I” of the fund invested primarily in notable national leaders in semiconductor manufacturing (SMIC, Huahong, Silan, Sanan), design (Analogix, Goodix), and packaging & testing companies (JCET). In 2019, “Phase II” of the fund raised 204.5 billion RMB. The timing coincides with the United States’ export sanctions towards SMIC and key telecommunications equipment and manufacturers like Huawei and ZTE, depriving them of semiconductor equipment and advanced node semiconductors. This made salient the fact that the Chinese electronics and semiconductor supply chain still relied critically on foreign manufacturing equipment and advanced manufacturers. In contrast to Phase I, Phase II continues to extend equity subsidies to capital-intensive manufacturing firms, but support previously given to IC design firms was instead directed towards equipment and materials suppliers.

On March 20, 2018, the Ministry of Finance along with other authorities promulgated “[On Issues Concerning the Enterprise Income Tax Policies for Integrated Circuit Manufacturing](#)

[Enterprises](#)”,³⁷ replacing the 2011 tax incentives.

The strength of the tax incentives is contingent on the technology process and age of the firm. Firms that have operated for over 10 years with line width technologies <130nm get 2+3 tax break, with those with <65nm and >15 years get 5+5 tax break. Conditioning tax breaks on years of operations means that only established players such as SMIC and Shanghai Huahong/Huali [get the preferential treatment](#).³⁸ On August 4, 2020, the State Council unveiled yet [another major set of tax incentives](#)³⁹ to comprehensively exempt corporate income tax and import duties across sectors, covering now not just manufacturing but software, design, equipment, materials, packing & testing firms. Manufacturing projects with processes less than 28 nanometers with operating period of more than 15 years now enjoy 10 years of exempted income tax, while those between 28 and 65 nanometers have 5 years exemption with 5 years of halved taxes. The standard 2+3 tax break was awarded to manufacturing firms with technologies between 65 and 130 nanometers as well as design, packaging & testing, equipment, and materials companies, with designated key IC design also getting a five-year exemption. This cemented the IC industry’s status as a national priority, with state support now officially extended throughout all segments of the semiconductor supply chain.

Table 2: Major Chinese Semiconductor Tax Incentives (adapted from [Song & Wen \(2023\)](#)⁴⁰)

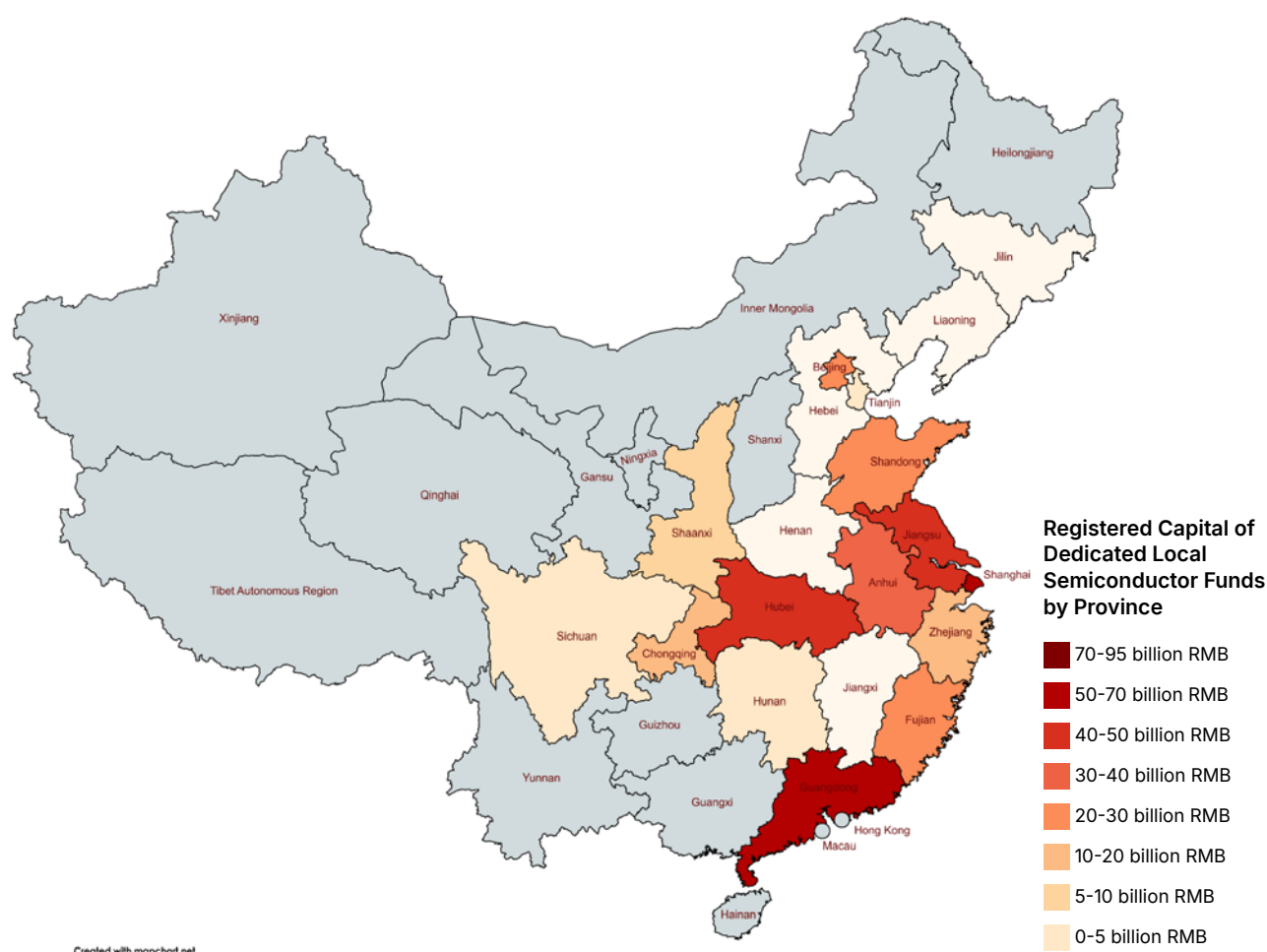
	Jan 2000: Several Policies to Encourage the Development of the Software Industry and IC Industry ("Document No.18")	Jan 2011: Several Policies to Further Encourage the Development of the Software Industry and the Integrated Circuit Industry ("Document No.4")	March 2018: "On Issues Concerning the Enterprise Income Tax Policies for Integrated Circuit Manufacturing Enterprises"	2020: Notice on Several Policies to Promote the High-Quality Development of the Integrated Circuit Industry and Software Industry in the New Era. ("Document No.8")
Value-added tax	VAT > 3% shall be "refunded immediately after collection" for ICs and software.	Special measures to solve financial problems encountered in major projects		
Import Duties	Import duties and value-added tax are exempted for materials & equipment.	Import taxes re-implemented; expediting customs clearance services for qualified enterprises.		For ≤ 65 nm and specialty manufacturers with line width ≤ 0.25 μm , import duties and VAT for materials & equipment are exempted. For compound manufacturers and ≤ 0.5 μm advanced packaging and testing companies, import duties for materials & equipment are exempted.
Corporate income tax	Newly established IC design and manufacturing enterprises enjoy "2+3" (2 yrs 0% + 3 years 12.5% starting from the profit-making year)	≤ 0.25 μm (or $> 8\text{b}$ investment) and > 15 years manufacturers can enjoy "5+5"; ≤ 0.25 μm manufacturers get 15% preferential tax rate vs 25%; ≤ 0.8 μm manufacturers enjoy "2+3"; Newly established design enterprises will enjoy "2+3"	≤ 65 nm and > 15 years manufacturers can enjoy "5+5"; ≤ 130 nm and > 10 years manufacturers can enjoy "2+3"; ≤ 0.25 μm (or $> 8\text{b}$ investment) and > 15 years manufacturers can enjoy "5+5"; ≤ 0.8 μm manufacturers enjoy "2+3"	≤ 28 nm and ≥ 15 years manufacturers can enjoy "10-year exemption"; ≤ 65 nm and ≥ 15 years can enjoy the preferential policy of "5+5"; ≤ 130 nm and > 15 years manufacturers can enjoy "2+3"; IC design, equipment, material, packaging, testing and software companies enjoy "2+3"; Key IC design enterprises are exempted for 5 years and get preferential 10% in subsequent years

In 2022, the Big Fund came under [an anti-corruption](#)⁴¹ probe in which many executives of Sino IC capital, including its [former CEO Ding Wenwu](#)⁴², were investigated and detained.

This partly reflected the central government's dissatisfaction with the fund's investment outcomes: some of the fund's portfolio firms had poor performance, most notably the conglomerate Tsinghua Unigroup that went bankrupt in July 2021 after a spree of semiconductor investments and acquisitions including chip designer UNISOC (formerly Spreadtrum) and NAND Flash maker YMTC. Consequently, the Big Fund stayed dormant for months before resuming operations in early 2023. "Phase III" of the Big Fund was quietly established on 24 May 2024 with 344 billion RMB of registered capital. Shareholders include the Ministry of Finance, central government banks and SOEs, and guidance funds/SOEs of Beijing, Shanghai, and Guangdong. Notably, apart from the aforementioned three major clusters of China's semiconductor industry, participation from other provincial governments was absent, while in the previous two phases localities like Fujian, Wuhan, Jiangsu, Anhui, and Chongqing have actively participated. This could reflect a desire to strengthen central control ⁴³ of Big Fund's investments, as equity participation from local governments would require the Big Fund to return favors by investing in local firms. So far no actual firm has received official investment from the fund, as the fund has adopted a "fund of funds" approach by dividing its portfolio to three subfunds, with one fund apparently dedicated to the artificial intelligence industry.

Local Government Policies: Cost & Performance-Based Subsidies, Equity Investments, Infrastructure Parks

Figure 3: Provincial Semiconductor Funds
(Number shown in 1 billion units) (Source: Qichacha & [Guoxin Securities](#)⁴⁴)



The central government conducts major tax cuts, promulgates general policy guidelines, and makes discretionary equity investments via the Big Fund and other central government guidance funds like [China Internet Investment Fund](#)⁴⁵ and [National Fund for Technology Transfer and Commercialisation](#)⁴⁶. Still, much of direct subsidies and equity investments originate from provincial and municipal

governments, who fund numerous government guidance funds with local fiscal revenue and debt. Shanghai and Shenzhen in particular pioneered the government venture capital model. The most successful government venture capital firm is the [Shenzhen Capital Group \(SCGC\)](#)⁴⁷. Established in 1999 and with total assets under management amounting to 489 billion RMB, it has invested in over

1580 companies and saw 272 portfolio firms go public. Focusing on investing in small and medium-sized young companies in emerging technology industries, the Shenzhen Capital Group has invested in semiconductor firms including SMIC, Empyrean, Montage, Biwin Storage, and Rockchip that have since become publicly listed. SCGC was named Top 1 VC firm in China from 2016-2024 by [Zero2IPO](#)⁴⁸.

Shanghai instituted Shanghai Technology Venture Capital in 1992 with 150 million RMB to focus on integrated circuits, biomedicine, and AI early-stage companies. With an AUM of 88.6 billion RMB, it has supported 102 firms getting listed on Shanghai Stock Exchange Sci-Tech innovation board or the STAR market. Notable semiconductor firms invested include AMEC, ACM Research, Enflame, Silergy, and 3Peak. Beijing E-town Capital was established in 2009 to primarily invest in targets in the Beijing Economic-Technological Development Area, an industrial park that became a cluster for semiconductor manufacturing in Beijing. Its mother fund and sub-funds now sprawl over 600 billion RMB. Apart from being a major investor of the Big Fund throughout Phase I to Phase III, it has supported various critical projects including display panel maker BOE's Beijing line, SMIC Beijing's Phase II and III 28-14nm fabs, and CXMT Beijing. It also has participated in Chinese entities' acquisition of foreign semiconductor firms, including automotive/industrial memory maker Integrated Silicon Solution Inc., Swedish MEMS maker Silex, American etching and thermal processing equipment supplier Mattson Technology, and American mixed signal designer Omnivision. Per the author's calculations, the total sum of local government equity investments in semiconductor firms exceeded that of the central government prior to the 2nd phase of the Big Fund (Figure 3).

Following the promulgation of the 2014 National IC Industry Development Promotion Outline, local governments at the provincial and municipal levels also instituted government guidance funds dedicated to investing in semiconductor firms locally. In the [Yangtze Delta region](#),⁴⁹ China's most vibrant semiconductor manufacturing cluster, at the provincial level Shanghai established a series of IC funds in 2015, including a dedicated IC manufacturing fund with a target size of 30 billion RMB, an IC design fund of 10 billion RMB, and a 10 billion fund dedicated to equipment and materials. Anhui in 2017 established a 30-billion RMB provincial IC fund, while at the municipal level Hefei introduced a 10-billion RMB manufacturing fund in conjunction with a 1 billion RMB IC design fund in 2015. In [Jiangsu](#),⁵⁰ Wuxi (10b), Nanjing (5b RMB), and Suzhou (5b RMB) each had deployed IC funds. In other major semiconductor clusters, Beijing allocated 32 billion RMB also to IC funds dedicated to advanced manufacturing, equipment, and design, packaging & testing. Similarly, Guangdong (15b) and key city [Guangzhou](#)⁵¹ (10b), [Hubei and its primary city Wuhan](#)⁵² (30b), Sichuan (12b), Fujian (50b), and Shaanxi (30b) have established numerous dedicated IC funds. The flurry of enthusiastic local government IC investments had mixed results as many high-profile projects eventually went bust such as [Wuhan Hongxin](#)⁵³ and [Tacoma](#)⁵⁴. These disappointments led to [concerns](#)⁵⁵ that this rush of local government funding has resulted in misallocation of critical fiscal resources as funding was dissipated across many regions in uncompetitive ventures.

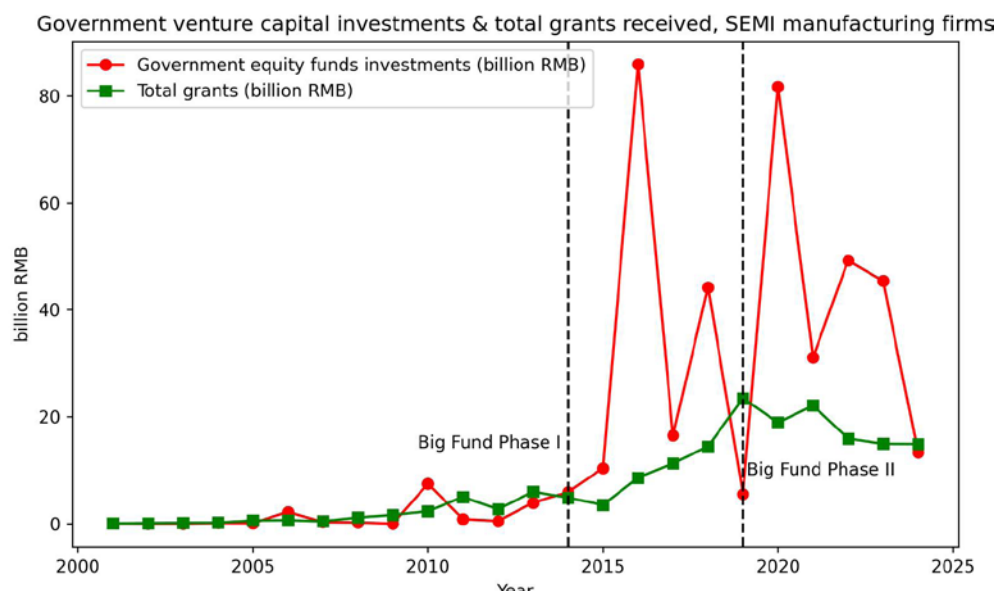
Apart from funding firms through equity injections, local governments also directly

provide grants to eligible firms via announcing specific measures targeted towards the IC industry. Summary analysis of more than 200 policy documents implemented by provincial, municipal, and sub-municipal documents suggests that policy measures across regions exhibit a high degree of similarity.⁵⁶ A common feature across localities is that they focus on subsidizing IC design firms' fixed costs of design: EDA software and IP costs as well as [photomask and tapeout costs](#)⁵⁷. Policies ubiquitously set the maximum percentage (typically less than 50%) of the fixed costs of EDA/IP/photomask/tapeout with a grant ceiling per applicant. Other commonly seen policies include cost-based R&D subsidies and equipment/materials subsidies that directly subsidize a percentage of the costs, as well as performance-based subsidies that award grants to firms based on fixed percentage of their sales, capital investment, or R&D outcomes such as patent counts. Other policies include subsidies to firms that relocate from other localities, and subsidies to firms that acquire other firms.

Shenzhen's "[Measures for Promoting High-Quality Development of the Semiconductor and Integrated Circuit Industries](#)"⁵⁸ exemplifies a typical set of such policies. For design firms' fixed costs, the policy subsidizes a maximum 20% of core IP procurement cost and 70% of the cost of purchasing domestic EDA tools. It also covers a maximum 50% of photomask cost and 70% of the tapeout cost of firms that are introducing a product with a full-mask tapeout for the first time. On capital and R&D investment, it subsidizes 10% of the capital investment cost of advanced packaging firms, 20% of the R&D cost of firms engaging in RISC-V designs and 40% of material firms' R&D cost. In addition

to subsidizing costs ex-ante, the policy also includes performance-based incentives, such as awarding firms that sold over 20 million RMB of a single compound semiconductor product to Shenzhen firms a maximum of 20% of that year's sales and awarding 30% of first-time sale of materials and equipment to key manufacturing firms. For firms that exceeded each level of sales benchmark, the management team of that enterprise would also receive a one-time bonus of a different amount. Figure 4 plots both subsidies and government equity capital for manufacturing firms that report subsidies from their earnings report or from the National Bureau of Statistics (NBS) manufacturing surveys. Across years, manufacturing firms received approximately a similar amount of subsidies and government equity injections before 2010. The financial crisis saw new equity investments plummeting to zero in 2009 before sharply rebounding in 2010. Since then, equity investment has become the primary means by which Chinese governments distribute funds to semiconductor manufacturers with fabs. In particular, government guidance fund and venture capital activity spiked after 2014, a consequence of the announcement of the Big Fund and related policies. Around the same time, the State Council announced "Notice on Cleaning Up and Regulating Preferential Policies such as Tax Incentives" (Document No. 62), regulating local governments to not promulgate unilateral preferential tax and fiscal policies without explicit authorization of the State Council. This further induced local governments to shift fiscal resources from subsidies and tax breaks to guidance funds/venture capital, through which support to firms could be recognized as assets on governments' balance sheets rather than liabilities. Annual flows of equity capital relative to grants to manufacturers thus have widened since 2015.

Figure 4: Manufacturing Firms: Subsidies and Government Equity for Manufacturing Firms Across Years (Source: Qichacha and National Bureau of Statistics Manufacturing Surveys, 1998-2011)



Local governments also supply infrastructure, land, and energy to build industry clusters via the creation of special economic zones and industrial parks. Similar to the spirit of Taiwan's Science Parks, Chinese industrial parks exploit the agglomeration economy of firms along the electronics supply chain. By securing large-scale investments of key manufacturers through discretionary subsidies and equity joint ventures, these major project investments attract further investments from smaller-scale upstream equipment & materials suppliers as well as downstream IC design customers. Famous examples include Beijing Yizhuang, Wuhan Optics Valley, Wuxi Gaoxin, and Hefei Hi-tech Park that host the pillar semiconductor firms of the region as well as nascent startups. Authorities managing the parks attract firms through favorable loan policies, expediting land acquisitions and construction, creating office and residential space to attract talent, and funding public goods such as common software/IP platforms, joint R&D efforts, and industry fairs.

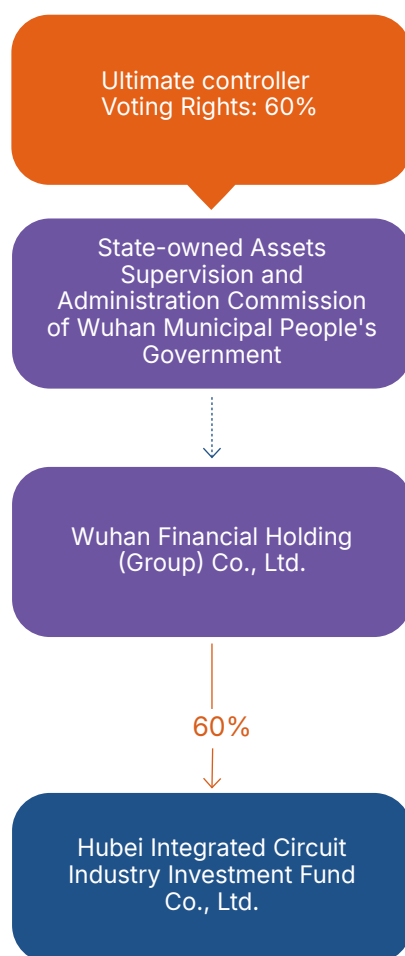
Following the Big Fund crackdown and reorganization, the Central Science and Technology Commission (CSTC) was established within the Chinese Communist Party with the intent for the CSTC to take over the strategic planning and agenda setting of science and technology policy. Commentators have suggested that this reflects the central government's desire to centralize and coordinate national R&D and industrial resources to focus on critical sectors and firms. CSTC's 2023 Notice on Management Measures for Central Guidance Funds for Local S&T Development stipulates that central government guidance fund investment will [prioritize](#)⁵⁹ (1) CSTC-approved major science and technology projects in need of central financial support and (2) regional science and technology innovation ecosystems, which are also now being [reviewed and approved](#)⁶⁰ by the CSTC. This represents a significant step by which the central government is now actively stepping in to coordinate local policies to avoid wasteful misallocation of subsidies and temper the excessive capacity competition between localities.

Data and Descriptive Facts

To document Chinese government equity investments, I utilize Chinese business registration data from business intelligence platforms [Qichacha](#) and [Tianyancha](#), which contain shareholder, shareholder paid capital, and patent/intellectual property information of the universe of firms in China across its history. This enables me to track the immediate shareholders of firms, their equity share, and paid capital contributions across time, as well as that of the shareholders of the corporate shareholders, and so on. To identify whether a

given investment fund or partnership is a government fund and which government is the ultimate owner of the fund, for each corporate shareholder the data platform identifies the owner of the fund via shareholding or voting rights. With this feature I am thus able to identify whether a given government investment fund is owned by a central government entity (typically State Council, Ministry of Finance, or State Council SASAC) or a provincial/municipal government entity (provincial/municipal people's government, provincial/municipal SASAC).

Figure 5: Ultimate Controller of Hubei Integrated Circuit Industry Investment Fund Co., Ltd Is Wuhan People's Government State-Owned Assets Supervision and Administration Commission (SASAC)(Source: [Qichacha](#))



For manufacturing outcomes in the semiconductor industry, I rely on [SEMI's](#)⁶¹ global semiconductor plant (fab)-level data on capacity, investment, product & process technologies (1996-2024). The SEMI fab-level data has quarterly estimates of each known semiconductor wafer fab's capacity and investment (\$ US million) in equipment and construction, as well as the fab's product offerings, technology process node, and wafer size each quarter. According to SEMI, the capacity and spending estimates are from company contacts as well as various industry sources such as "news articles, capital spending plans, earning reports, SEC filings, presentations, announced fab plans, ramp schedules, and technology roadmaps." It also utilizes its network of equipment suppliers and uses their billing information to update and adjust quarterly data. As Chinese manufacturers still primarily rely on equipment manufactured by leading companies in the US, the Netherlands, and Japan, the equipment spending estimates constitute a reliable metric of Chinese fabs' capital expenditures, which takes up the overwhelming majority of a fab's lifetime operating expenses .

As the SEMI data only covers capacity and capital expenditures, I supplement it with firm-level National Bureau of Statistics Manufacturing Surveys (2000-2011), which contain survey outcomes for all Chinese manufacturing firms with sales exceeding 5 million RMB . Apart from standard manufacturing survey items like sales, assets, employment, material inputs, wages, and profit, it also contains taxes paid and cash subsidies. Along with government equity holdings data, this information paints a comprehensive picture of the money support

semiconductor firms received from the government before 2011. For publicly listed semiconductor firms, detailed firm-level financials and production data are obtained from earnings report and China-focused financial databases such as CSMAR and Wind. Publicly listed firms also report the subsidies they received from the government quarterly.

To document price trends, I utilize Global Semiconductor Alliance (GSA)'s [Wafer Fabrication and Assembly Pricing](#)⁶² dataset, which contains a quarterly survey sample of prices of different semiconductor wafers, the output of semiconductor manufacturers to be sold to fabless IC design firms, from 2012-2021. The dataset's buyer and seller identities are anonymized and only the location of the foundry is known along with the order quantity and technological characteristics such as nanometer node, wafer size, and the number of mask layers. With the aforementioned data, this section discusses several facts about the development of the Chinese semiconductor industry and government support since 1996.

Figures 6 and 7 show that across different process node groups and semiconductor product types, Chinese wafer production capacity has been rising in the SEMI data⁶³. In terms of the share of capacity globally, China now commands a significant position in mature node semiconductors of process nodes greater than 28nm, reaching 30% in 2024. It leads particularly in discrete and optoelectronics, though recently Chinese momentum in analog, MEMS, and logic has accelerated. The rise is a direct outcome of the acceleration of new fab construction in China as well as the amount of equipment spending. The vast majority of fab

lines in China is in <80 nm mature processes that are less capital-intensive (Figure 10), while Chinese equipment spending in 11-33nm (Figure 11), the middle ground between sum 10nm advanced processes and >34 nm MOSFET processes, has noticeably exploded since 2020. Chinese firms are now taking up the vast majority of the world's equipment spending (Figure 11).

Fact 1: Rising Chinese Share of Capacity and Equipment Spending

Figure 6: Chinese Wafer Capacity by Process Node Group (SEMI data)

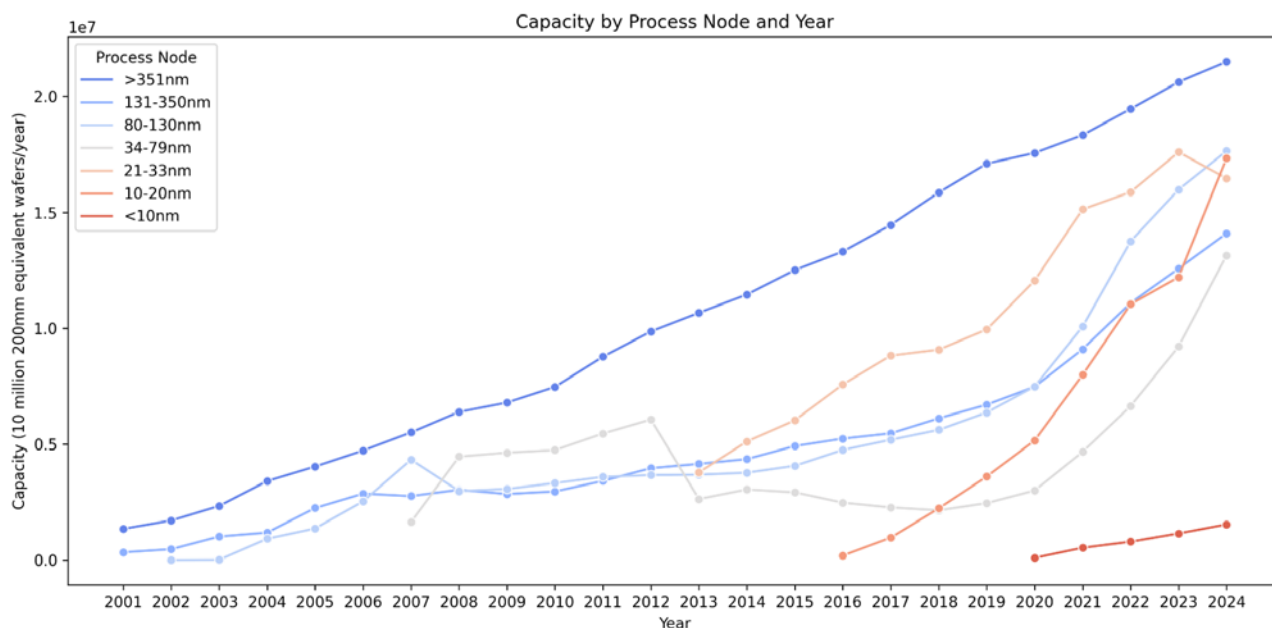


Figure 7: Chinese Wafer Capacity by Product (SEMI data)

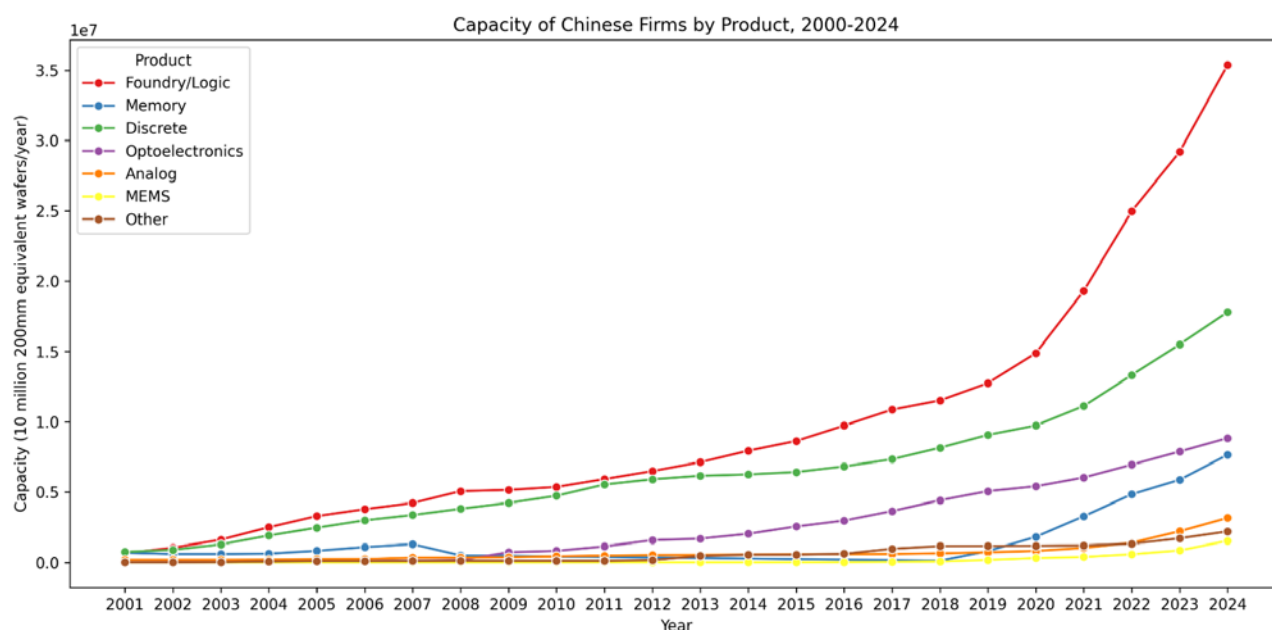


Figure 8: Chinese Wafer Capacity Share Globally by Process Node Group (SEMI data)

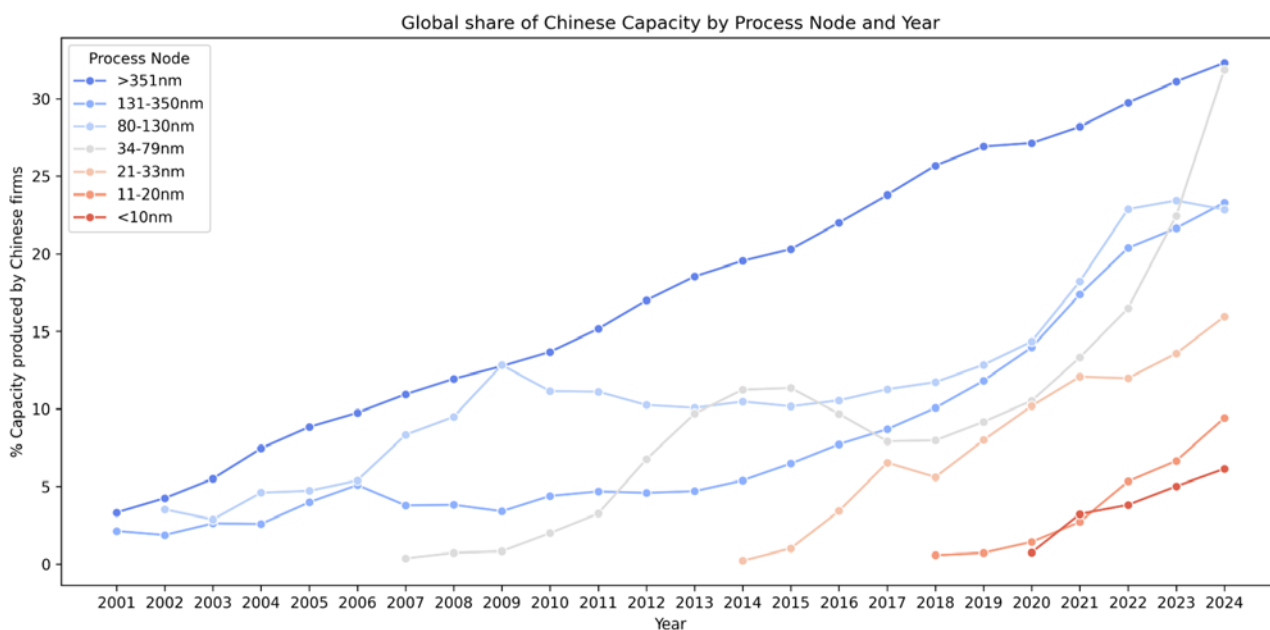


Figure 9: Chinese Wafer Capacity Share Globally by Product (SEMI data)

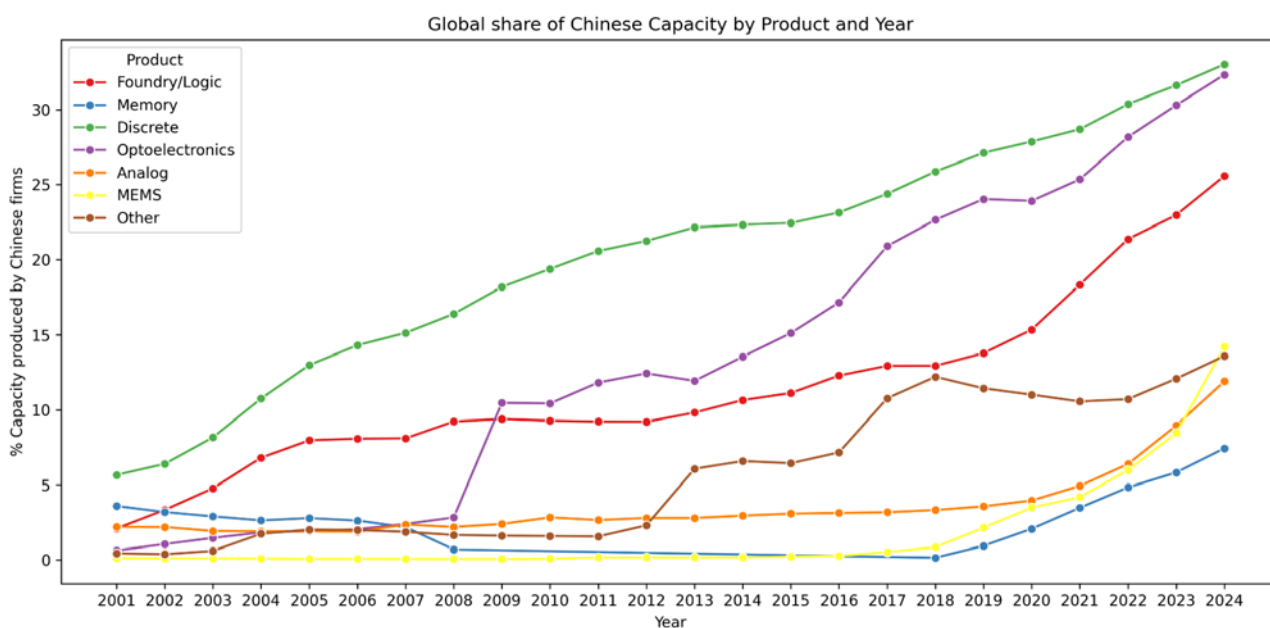


Figure 10: Number of Chinese Fab Projects (SEMI data)

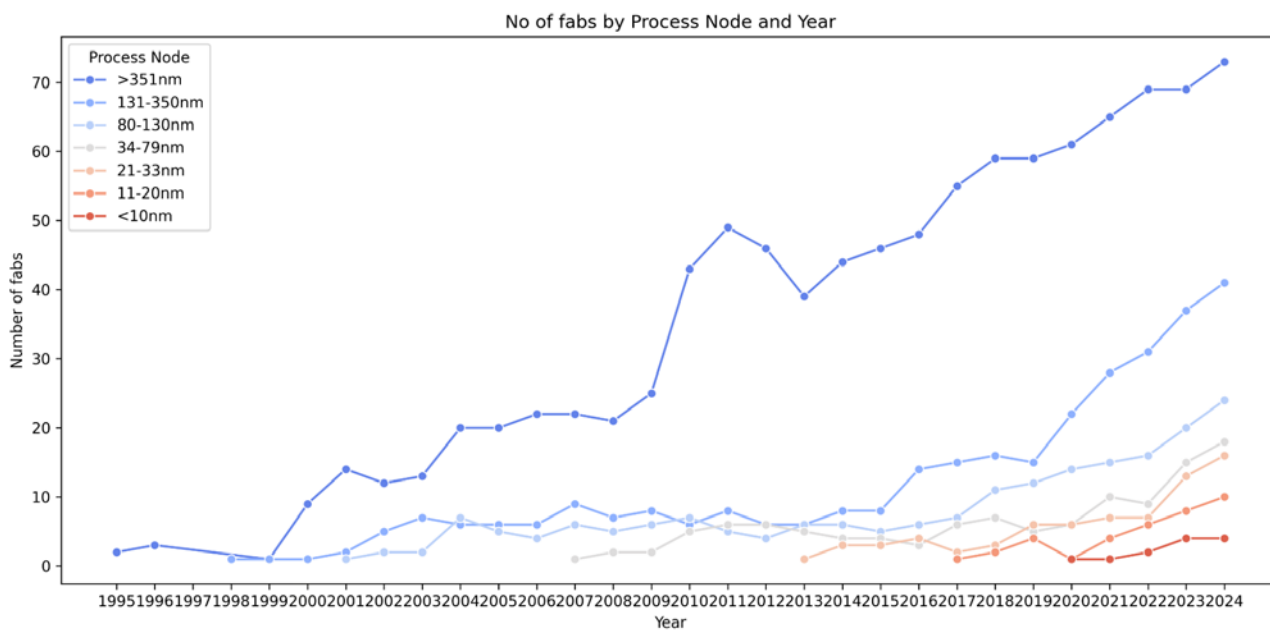
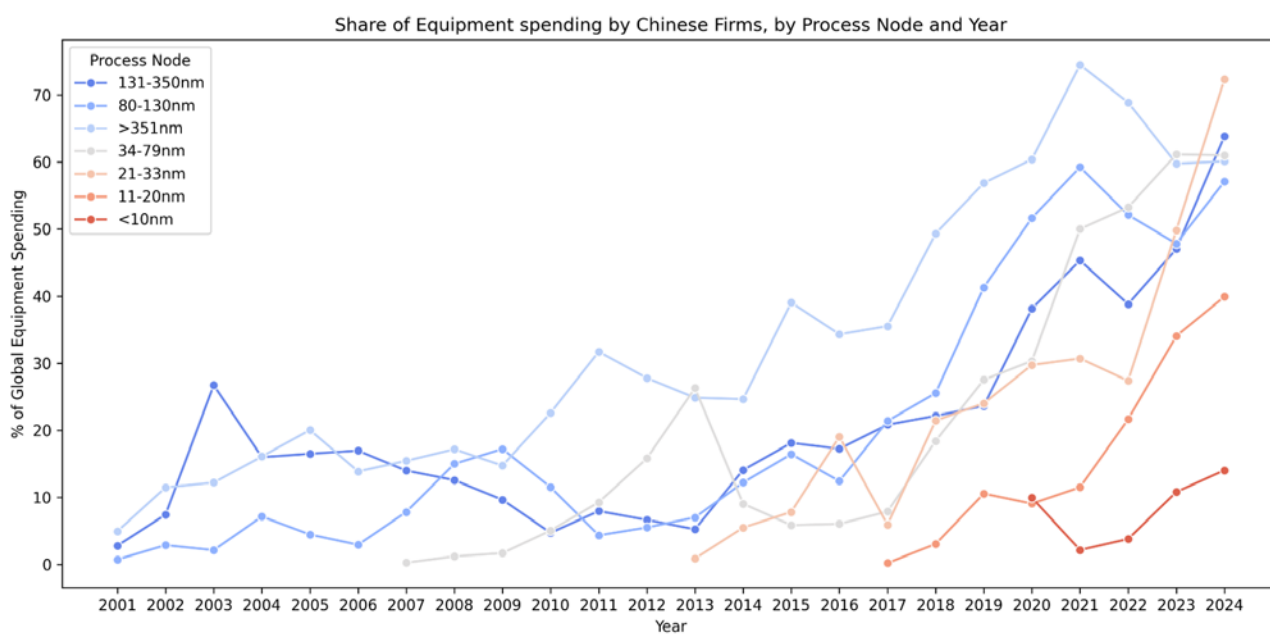


Figure 11: Chinese Equipment Spending (SEMI data)



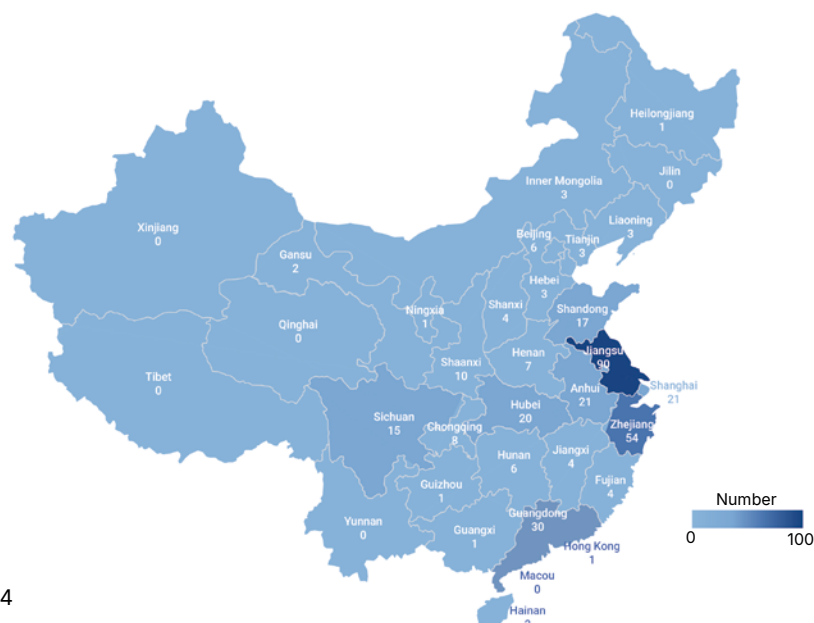
Geographic Dispersion of Plants, firms, and government subsidies

Semiconductor fabs are dispersed across Chinese provinces. Figure 12 counts the number of fab lines across provinces in 2023. By count the Yangtze River Delta region nexus of Shanghai-Zhejiang-Jiangsu has the overwhelming majority of fab lines, but sizeable numbers also exist in Guangdong, Hubei, Sichuan-Chongqing, Beijing-Tianjin, and Shaanxi. In terms of production (Figure 13)⁶⁴, Chinese government statistics again show that Jiangsu and Guangdong dominate the majority of IC production. Gansu is another major end-product producer of packaged ICs due to the presence of packaging giant Tianshui Huatian. Figures 14 and 15 plot central and local guidance funds' paid capital to semiconductor firms by province in 2024 respectively. The central government concentrated its investments in Beijing, Shanghai, and Hubei, while local governments in Fujian, Anhui, and Hubei expended considerable capital to promote local manufacturing.

Fact 2: Geographic Dispersion of Plants, Firms, and Government Subsidies

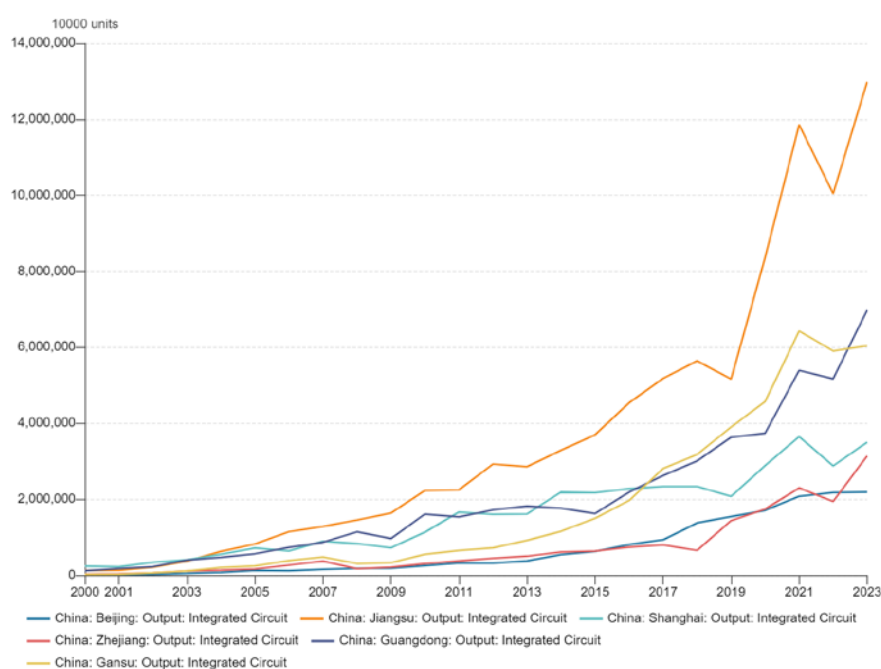
Figure 12: Number of Chinese Semiconductor Projects by Province 2023
(Source: [Trendforce](#)⁶⁵)

China's 2023 Semiconductor Projects Map



Source: TrendForce, Jan., 2024

Figure 13: Integrated Circuits Output by Province (Source: National Bureau of Statistics, Wind)



Source : Wind

Figure 14: Provincial Distribution of Central Government Equity Paid Capital in Semiconductor Firms, 2024 (10000 RMB) (Author's calculations)

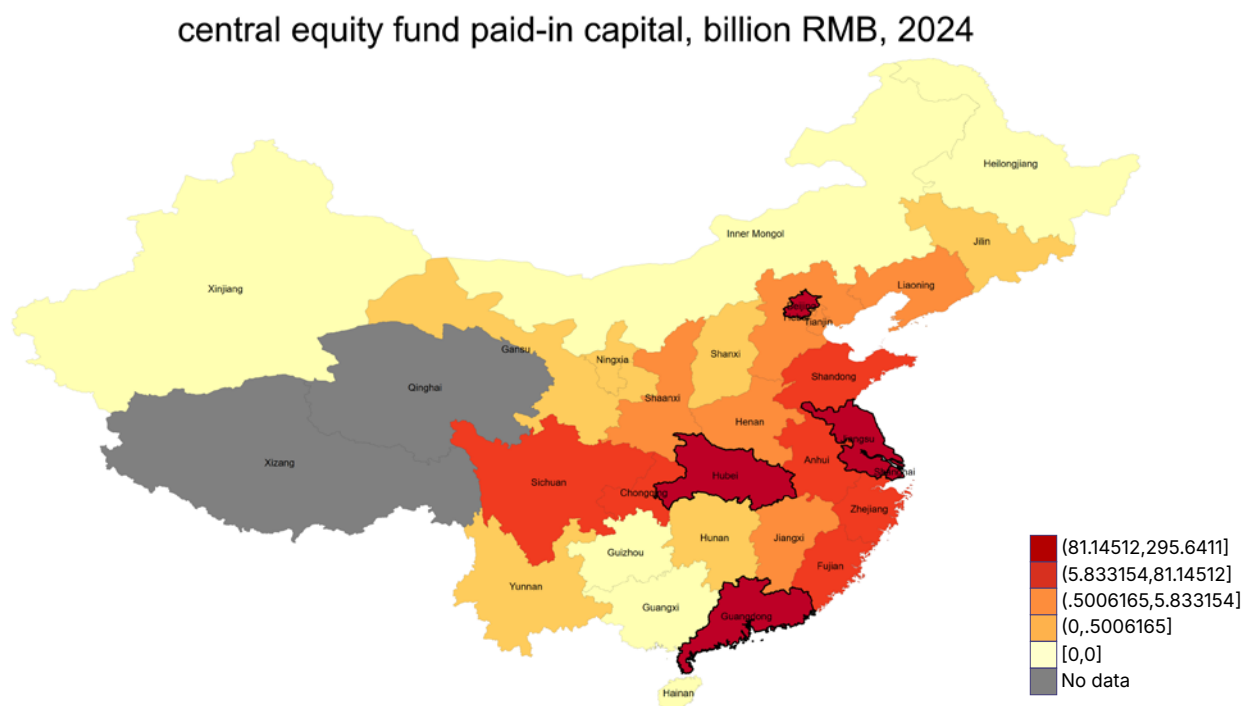
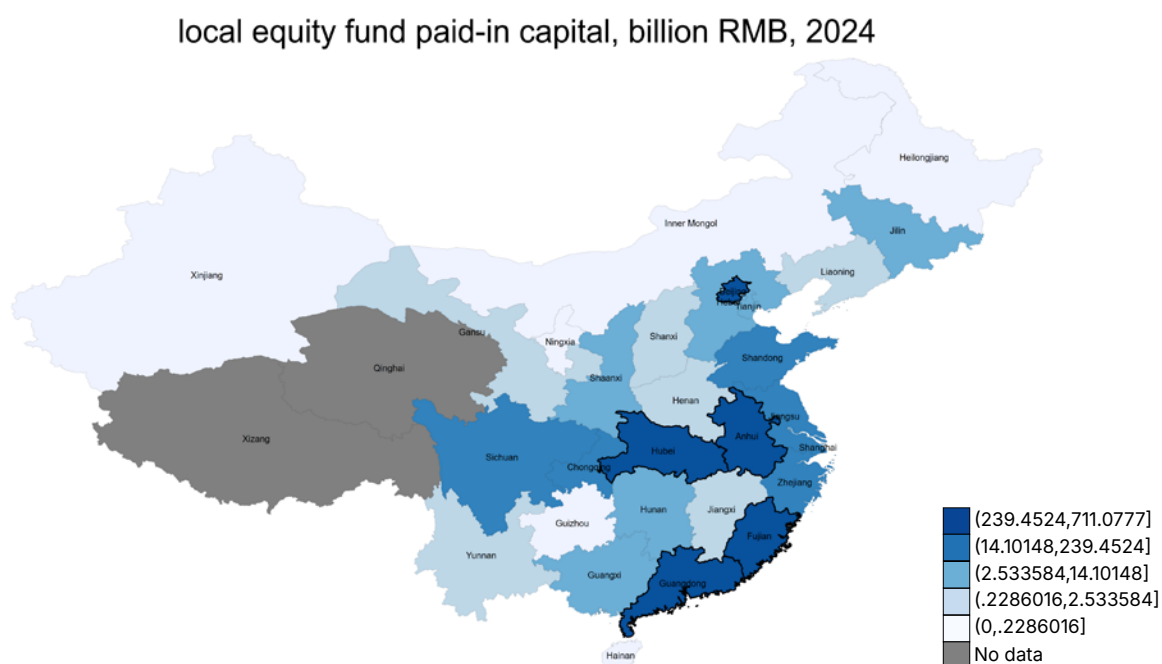


Figure 15: Provincial Distribution of Local Government Equity Paid Capital in Semiconductor Firms, 2024 (10000 RMB) (Author's calculations)



Fact 3: Local Equity Subsidies Preceded that of the Central Government

As Chinese local governments pioneered the government venture capital model, they started supporting the semiconductor industry in significant amounts early on. Figure 16 plots the sum of shareholder paid-in capital across semiconductor firms in China (across all subsectors) by the type of investor: central government funds in red, local government funds in blue, and foreign investors (including foreign firms, private equity, and venture capital) in green. Foreign investments have had a significant presence in China since the early 2000s. Local governments actively funded the industry prior to the entry of the Big Fund in 2014. Central equity funding spiked after the Big Fund's introduction in 2014. New waves of local government funds soon follow suit. Local governments remain the dominant force behind equity financing of semiconductor firms in China, with total equity stakes eclipsing that of foreign capital after 2016.

Figures 17 and 18 compare central and local government equity investments in various subsectors of the industry across years. Local governments are pioneers in investing in more mature subsectors such as optoelectronics, analog and discrete semiconductors, and assembly & testing. Central government efforts are directed to foundry/IDM firms as exemplified by the 908/909 project and later design firms. Local governments are also strong early supporters of the memory IDMs, and have ramped up support towards foundry/IDM, design, and equipment/materials along with central government directives.

As will be discussed later more in detail in Fact 4, firms that are jointly owned by a central government and a local government guidance fund only became increasingly common after the Big Fund in 2014. Before that, most government guidance fund-invested firms are either invested by a local fund or a central fund. At the firm level, I examine whether firms that are eventually jointly owned by both the central and local government exhibit different patterns by running the following event study regressions: The indicators $1(\text{central GF owned})_{it}$ and $1(\text{local GF owned})_{it}$ represent whether firm i is owned by a central or local GF at quarter t . The indicators $1(\text{first time central GF investment at quarter } t-k)$ and $1(\text{first time local GF investment at quarter } t-k)$ represent whether quarter t is k quarters ahead or after the event when the firm first receives equity investment from a local or central government guidance fund. X_{it} are controls including firm age and log firm total registered capital which represents firm size. Lagged dependent variables are controlled to account for serial correlation of equity ownership. δ_t and ρ_t are firm and time fixed effects respectively, with standard errors clustered at the firm levels. Thus the equations test whether local/central government fund entry predicts future central/local fund entry respectively.

Figures 19 and 20 plot the event study coefficients β_k for regression (1) and (2) respectively. The likelihood of a central government fund investment increases after a firm receives equity injection from a local government fund, while the opposite response from local government funds with respect to central government investment is more muted. This suggests that local government investment decisions generally precede that of the central government.

$$\begin{aligned} \mathbb{1}(\text{central GF owned})_{it} = & \sum_{k=-25}^{40} \beta_k \mathbb{1}(\text{first-time local GF investment at quarter } t-k)_{it} \\ & + \alpha \mathbb{1}(\text{central GF owned})_{it-1} + \gamma' X_{it} + \delta_i + \rho_t + \epsilon_{it} \end{aligned} \quad (1)$$

$$\begin{aligned} \mathbb{1}(\text{local GF owned})_{it} = & \sum_{k=-25}^{40} \beta_k \mathbb{1}(\text{first-time central GF investment at quarter } t-k)_{it} \\ & + \alpha \mathbb{1}(\text{local GF owned})_{it-1} + \gamma' X_{it} + \delta_i + \rho_t + \epsilon_{it} \end{aligned} \quad (2)$$

Figure 16: Local and Central Government Equity Investments vs. Foreign Equity Holdings in Chinese Semiconductor Firms (Log Billion RMB) (Author's calculations)

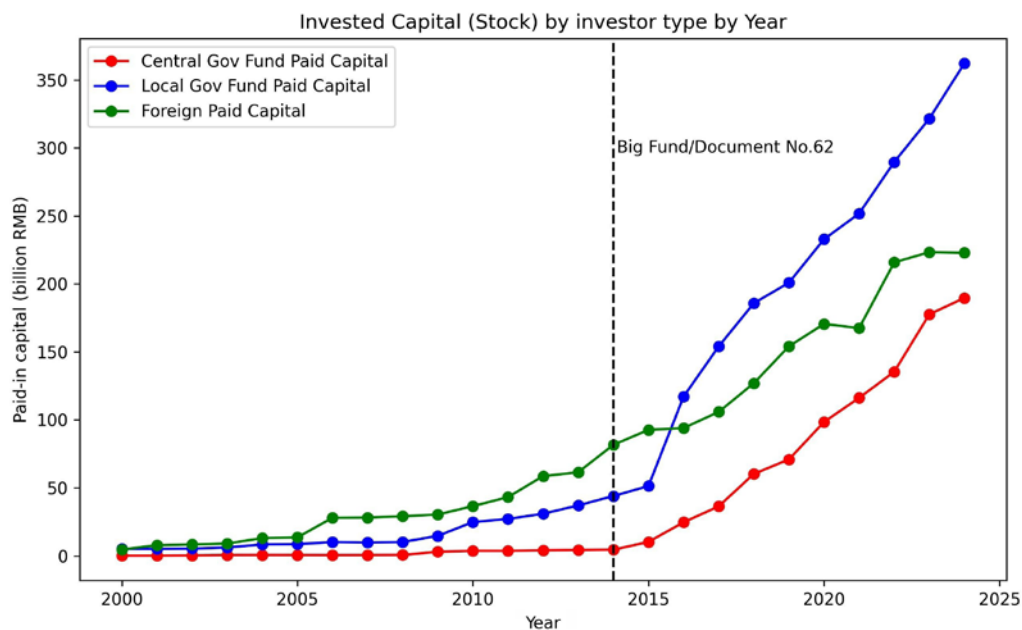


Figure 17: Central Government Equity Funding by Sector, All Semiconductor Firms

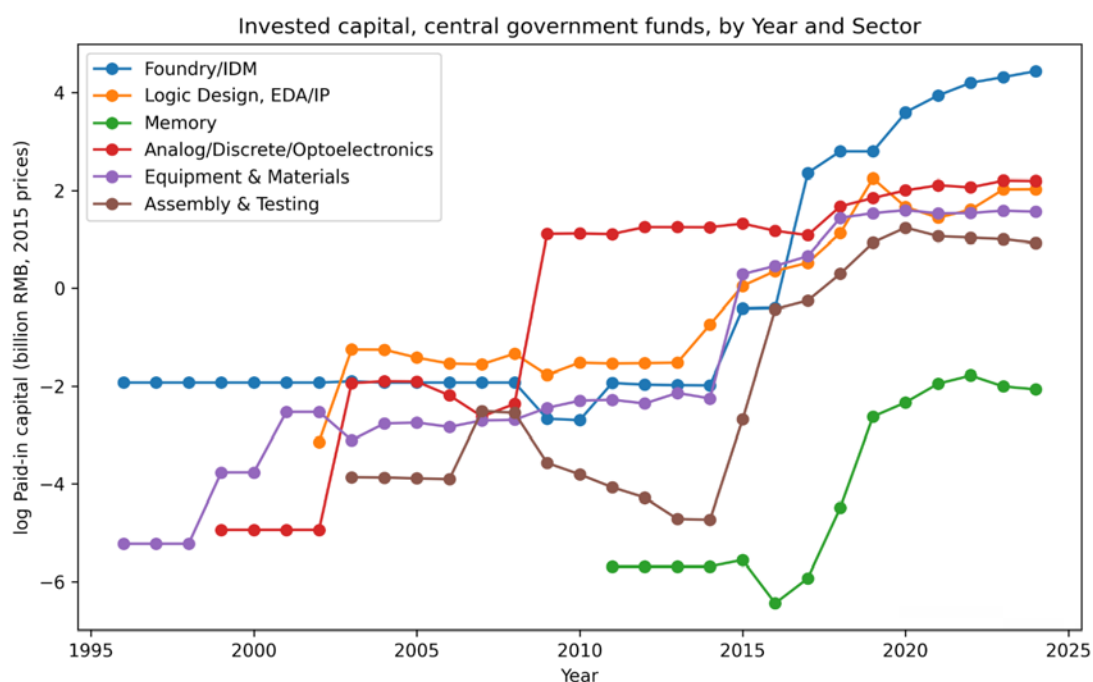


Figure 18: Local Government Equity Funding by Sector, All Semiconductor Firms

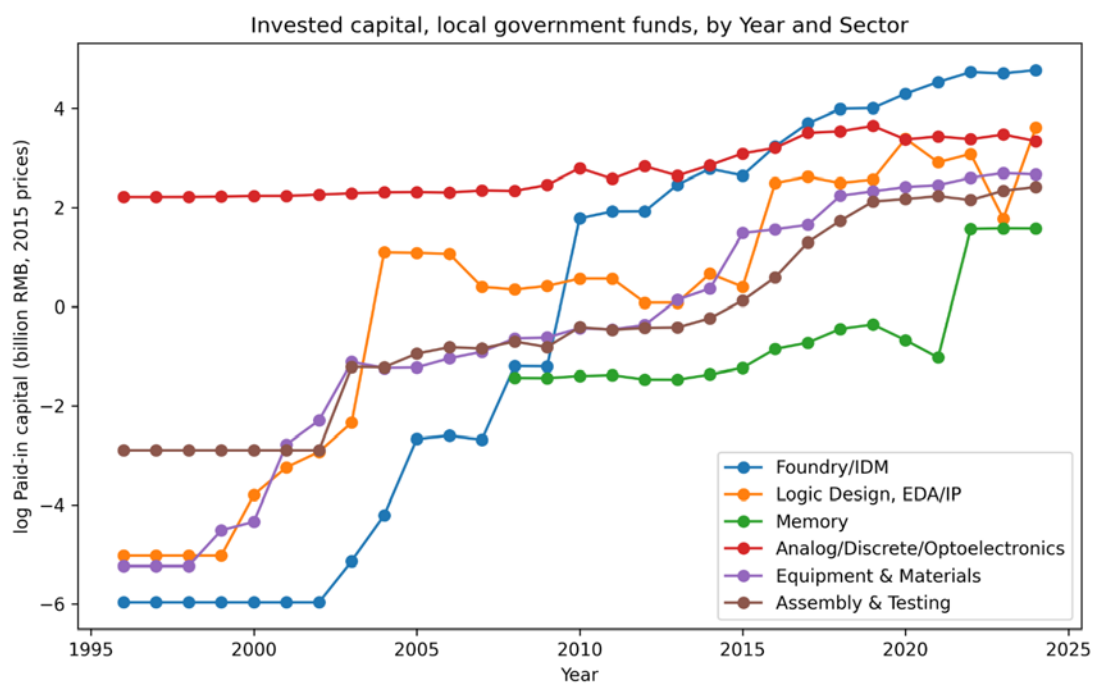


Figure 19: Change in Central Investment Probability Before and After Local GF Investment Event, Event Study Estimates

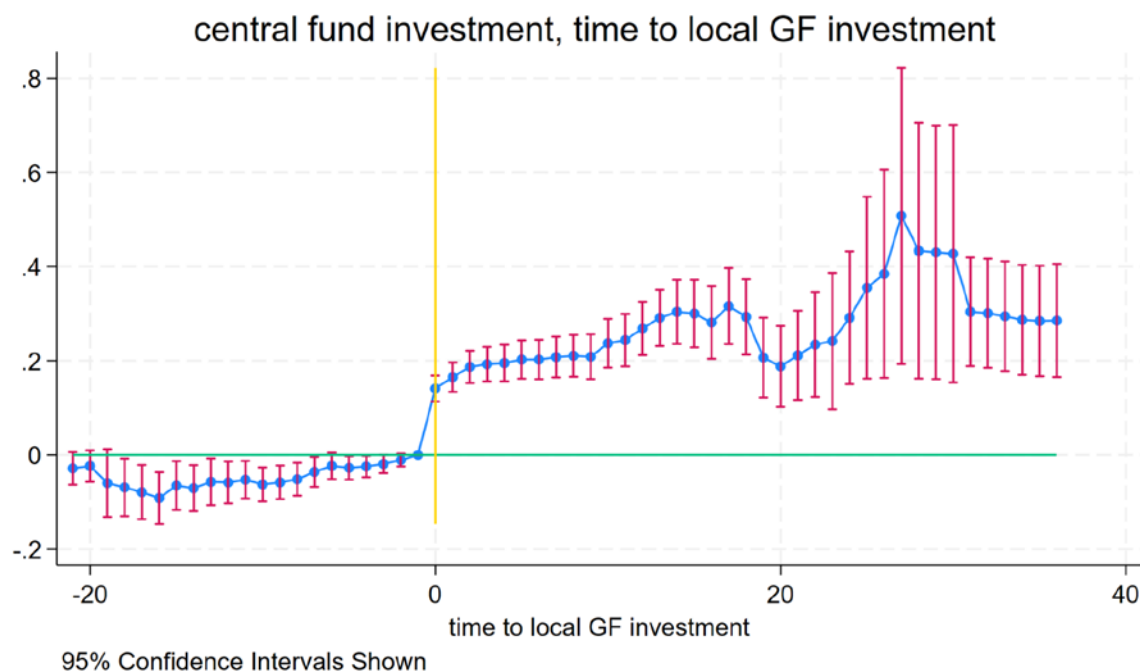
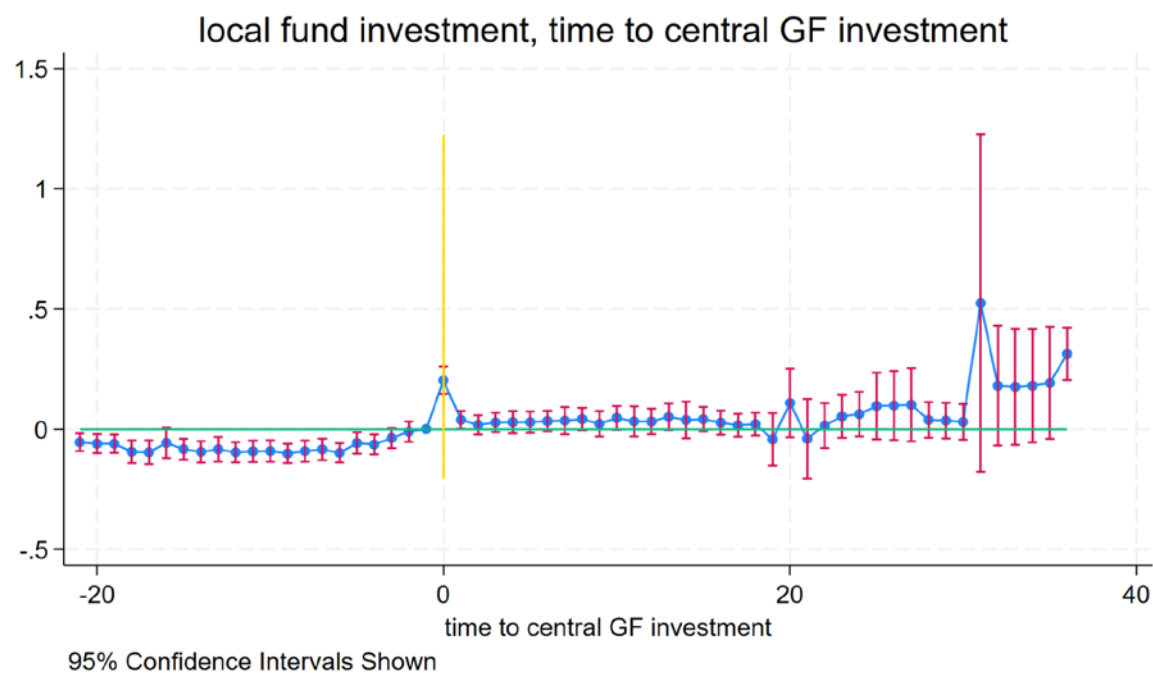


Figure 20: Change in Local Investment Probability Before and After Central GF Investment Event, Event Study Estimates



Fact 4: Substantial Variation in Capacity per Capital Stock

Chinese fabs, even within the same product and same technology node, exhibit wide variation in capacity per million dollar of capital investment. For each fab $\times$ quarter in full production, I compute the stock of capital in that quarter by summing up past equipment and construction expenditures and assuming capital depreciates in [20 years](#)⁶⁶ and building depreciates in [39 years](#)⁶⁷.

Figure 21 plots the distribution of log capacity (200mm wafer equivalents) divided by total capital stock within a broad process node group for fabs in 2024. The number of wafers produced per capital stock is decreasing for more advanced technology. We observe that within each process node group, there is wide variation in capacity per dollar of capital. Theoretically, if capacity depends only on equipment throughput and the number of equipment, and different firms face similar input prices on predominantly imported equipment, the variation in capacity per dollar of capital stock should not differ that widely. However, analysis by McKinsey suggests that managerial practices that [minimize equipment turnover time](#)⁶⁸, [regularly maintain tools](#),⁶⁹ and [maximize operator touch time](#)⁷⁰ could improve capacity without adding equipment. Thus the variation in capacity per equipment stock constitutes a measure of the variation in productivity that reflects managerial and organizational practices among Chinese fabs.

To further investigate the variation in capacity per capital stock by plants' ownership type,

I classify plants by whether their firms are invested by a local government guidance fund, a central government guidance fund, both types of guidance fund, a state-owned enterprise⁷¹, private firms, and foreign-owned firms. To compare productivities of plants producing different products and process nodes, for each plant in each year, I compute how many standard deviations above or below the mean capacity/capital ratio of plants in the same product $\times$ process node category is the plant's capacity/capital ratio. The paper will refer to this as a "z-score measure." A higher z-score measure indicates that the plant is of higher capacity productivity ranking relative to its peers in the same sector (defined as a semiconductor product in a process node group) globally.

Figures 22, 23, and 24 plot the distributions of plants' global capacity/investment z-score for each ownership type in each year. The horizontal axis plots the year, and within each year there are six box-and-whisker representing the distribution of firms' capacity/capital global z-scores within each six distinct ownership group: local government fund owned, central government fund owned, owned by both, SOE, private firms, and foreign-owned firms. The number below each box and whisker bar indicates the number of plants in that ownership category in that year. In the period 2006-12, only a few plants were invested by a central government fund, while a substantial number of plants were invested by local government funds or stayed private. Only after the entry of the Big Fund in 2014 did a substantial number of plants become invested by a central fund only. Notably, Chinese plants tend to be below the mean of their sectors' capacity/capital ratio globally (i.e. the z-scores tend to be lower than

0) except a few episodes: firms jointly invested by central and local funds have higher than global average capacity/capital ratio from 2006-13. Some SOEs have higher than global mean after 2018, which is a product of the entry of multiple national labs that have less investment relative to their capacity. It is not obvious that government guidance funds are investing in plants that are particularly productive given their capital stock, suggesting *prima facie* that there is substantial misallocation of government equity capital as many unproductive firms nationally receive local and central government injections.

In figures 25, 26, and 27, we redo the same exercise, but now the z-score reference group is not plants in the same sector globally but plants in the same sector within the province. It is now apparent that compared to plants in other ownership categories, local government funds invest in plants that have higher capacity/capital stock ratio relative to their provincial peers. Thus local government guidance funds, to the extent that their aim is to maximize semiconductor output and sales within their locality, are achieving their objective by allocating capital to more productive plants. From the central government's perspective, however, as the most productive plants in the province (i.e. the provincial champions) are not necessarily the most productive plants nationally, thus substantial reallocation of local resources to nationally most productive firms will further improve national capacity.

Figure 21: Average Capacity/Total Capital Stock by Process Node in China

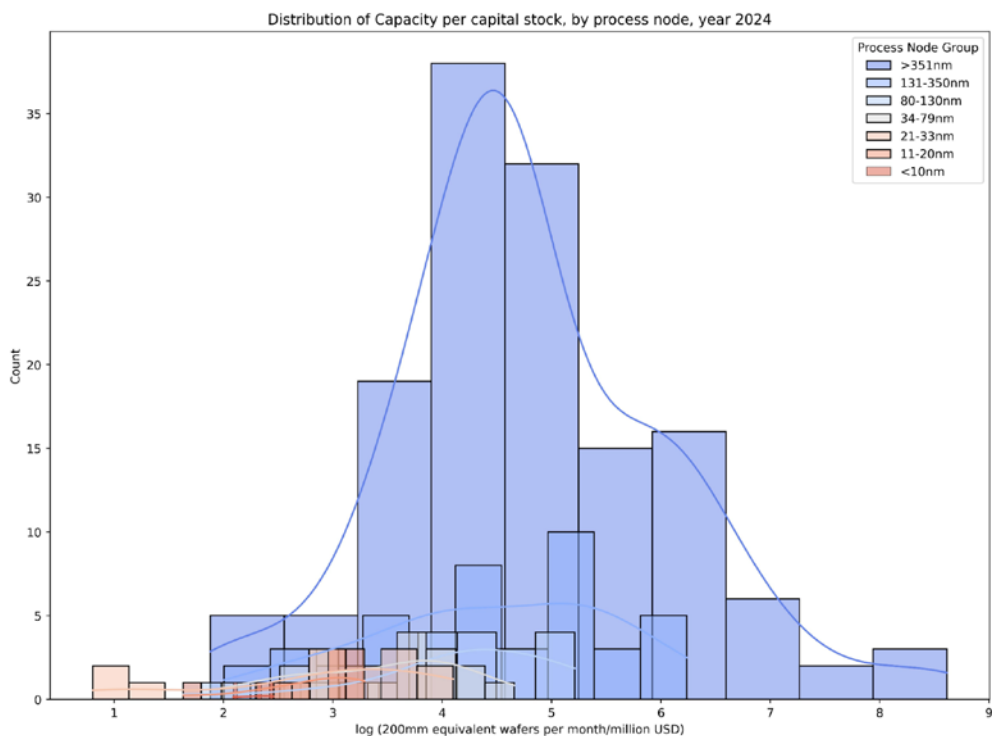


Figure 22: Average Capacity/Total Capital Stock Global Z-Score Distribution by Year and Ownership Type, 2006–12

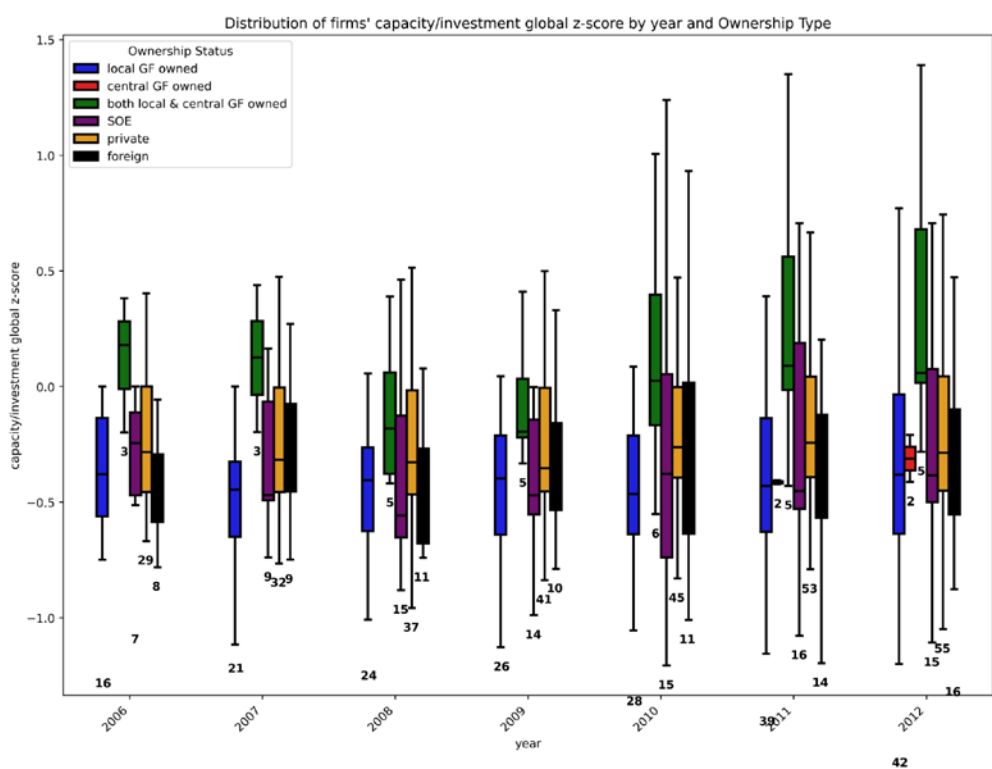


Figure 23: Average Capacity/Total Capital Stock Global Z-Score Distribution by Year and Ownership Type, 2013–18

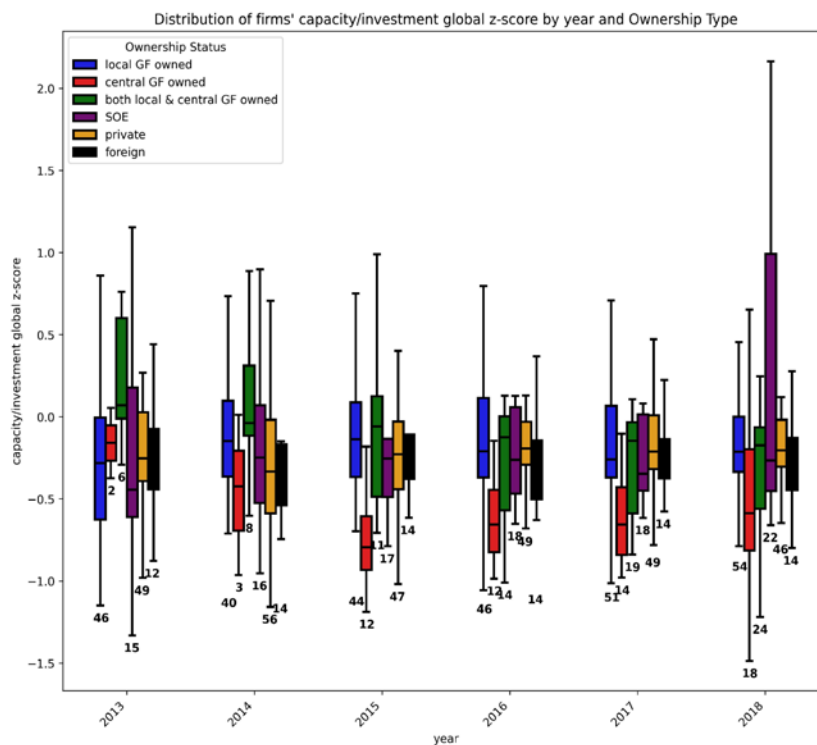


Figure 24: Average Capacity/Total Capital Stock Global Z-Score Distribution by Year and Ownership Type, 2019–24

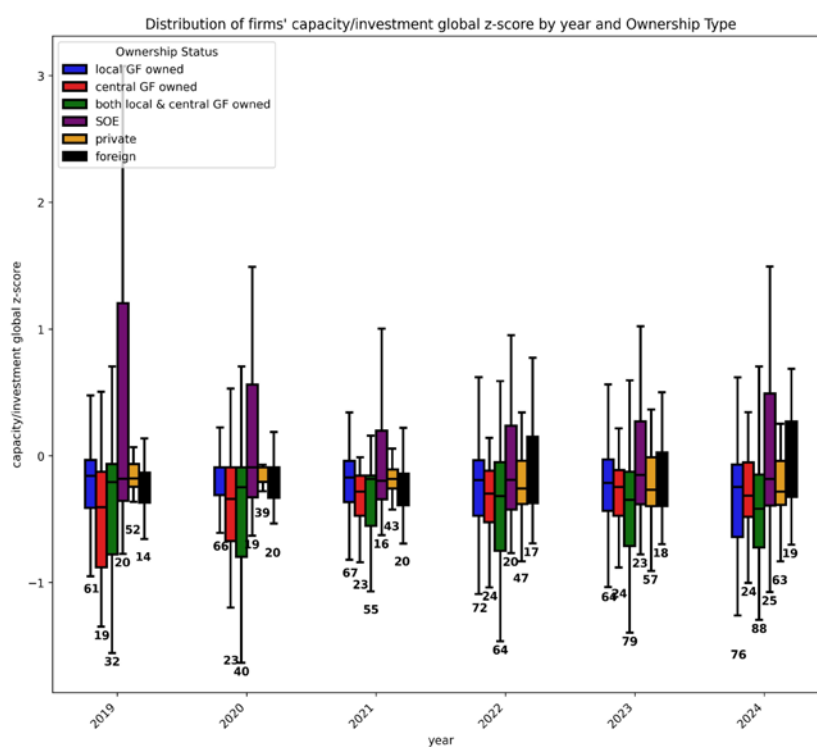


Figure 25: Average Capacity/Total Capital Stock Provincial Z-Score Distribution by Year and Ownership Type, 2006–12

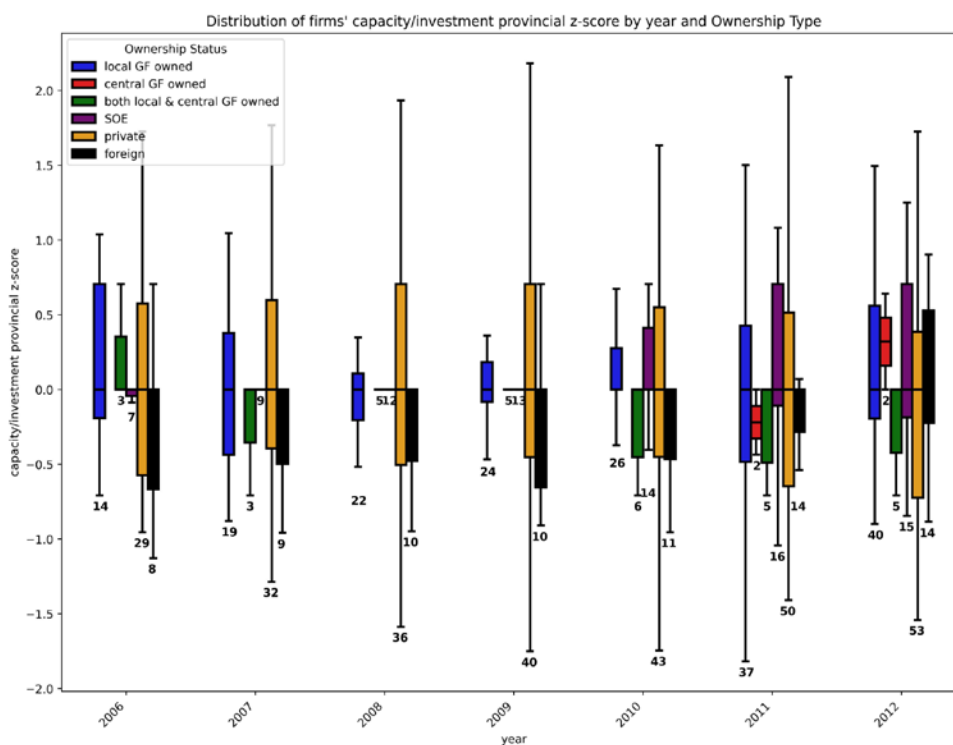


Figure 26: Average Capacity/Total Capital Stock Provincial Z-Score Distribution by Year and Ownership Type, 2013–18

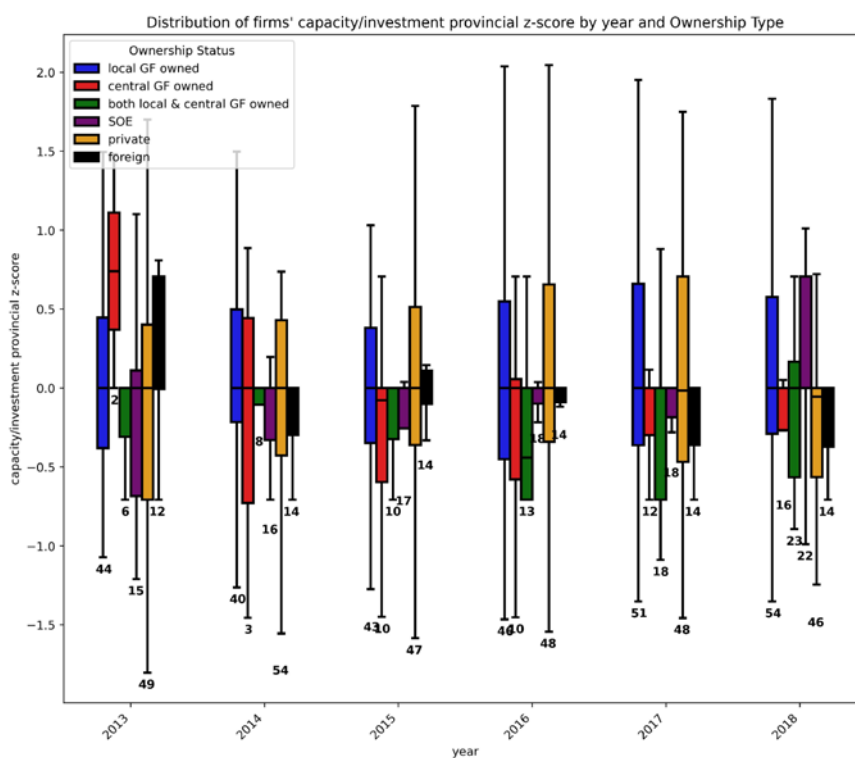
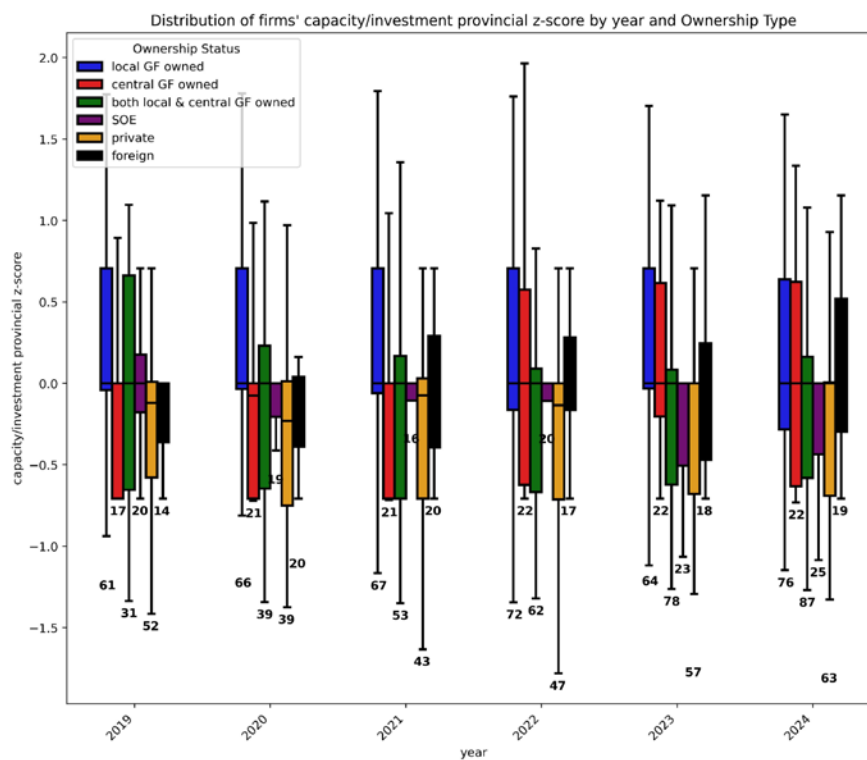


Figure 27: Average Capacity/Total Capital Stock Provincial Z-Score Distribution by Year and Ownership Type, 2019–24



Fact 5: Cheaper Chinese Wafer Prices

As a result of Chinese capacity expansion and heavy subsidies, Chinese firms are known to charge lower prices, especially in [mature node semiconductors](#)⁷² where Chinese yields are up to standard. Figure 28 plot the box and whisker plots of wafer prices (with wafer size normalized to 200mm equivalents) by broad process node categories: >130 nm, 81-130 nm, 41-80 nm, 29-40 nm, and <28 nm. As expected, within each year more advanced processes (smaller nm nodes) are much more expensive per wafer. Also across years, prices of mature nodes (<80 nm) appear stable while the advanced <28 nm nodes decrease over time. Figure 29 plots box and whisker plots of wafer prices of different process nodes by foundry location. The colored box indicates the range of prices from the 25th to the 75th percentile in the colored category in that particular year. We see that Chinese foundries generally charge lower prices, though Taiwanese prices are comparable. Lower Chinese prices are likely to be supported by equity, tax, and equipment cost subsidies discussed previously, resulting in less equipment depreciation cost per wafer from the perspective of a subsidized Chinese firm. Furthermore, as local governments seek to maximize local gross output rather than profitability of the firms in its equity portfolio, they are indifferent with respect to wafer prices and actually would prefer to see a competitive outcome of high production. Cheaper semiconductor inputs would be a boon to the costs of downstream IC designers and end product producers, which local governments also have stakes in. Fierce competition between Chinese manufacturers, each supported by

their local governments, further put pressure on Chinese wafer prices. As Taiwan lacks industrial policy of the scale and degree China has towards the industry, this made the competitive Taiwanese prices and market share in mature nodes more impressive. As supply chains increasingly bifurcated due to geopolitical realities, if non-Chinese IC designers and IDMs were to look for non-Chinese manufacturing alternatives, Taiwanese foundries are likely to be their preferred options.

Table 3 shows results from a regression of log per 200mm equivalent wafer prices on foundry location, year, and process node group fixed effects and other product characteristics such as the number of layers, masks, and log quantity of the order. Base category for the FEs is China, ≥ 350 nm group, and 2012. The positive coefficients significant at the 1% level on all locations suggest that controlling for product characteristics and year fixed effects, Chinese foundries have cheaper prices. Other coefficients correspond to the fact that more advanced process nodes are costlier, the same product's price decreases across time, and that per-unit prices increase with the number of layers and masks and decrease with the size of the order. The log-level regression coefficients suggest that Taiwanese wafers are about 11% more expensive than equivalent Chinese wafers controlling for quality characteristics like nanometer nodes and the number of layers as well as demand characteristics like the size of order (larger order gets lower prices per unit). Importantly, as this dataset does not have information on yields⁷³, another crucial piece determining the actual price per chip which Taiwanese manufacturers are known to excel in, this should reflect favorably on Taiwanese foundries' competitiveness.

Figure 28: Semiconductor Wafer Prices by Technology Node

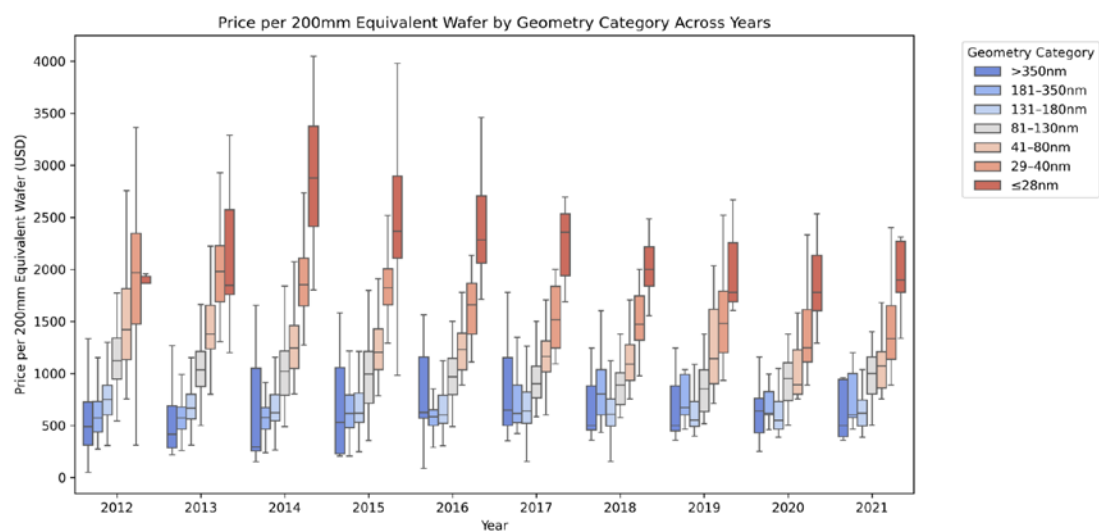
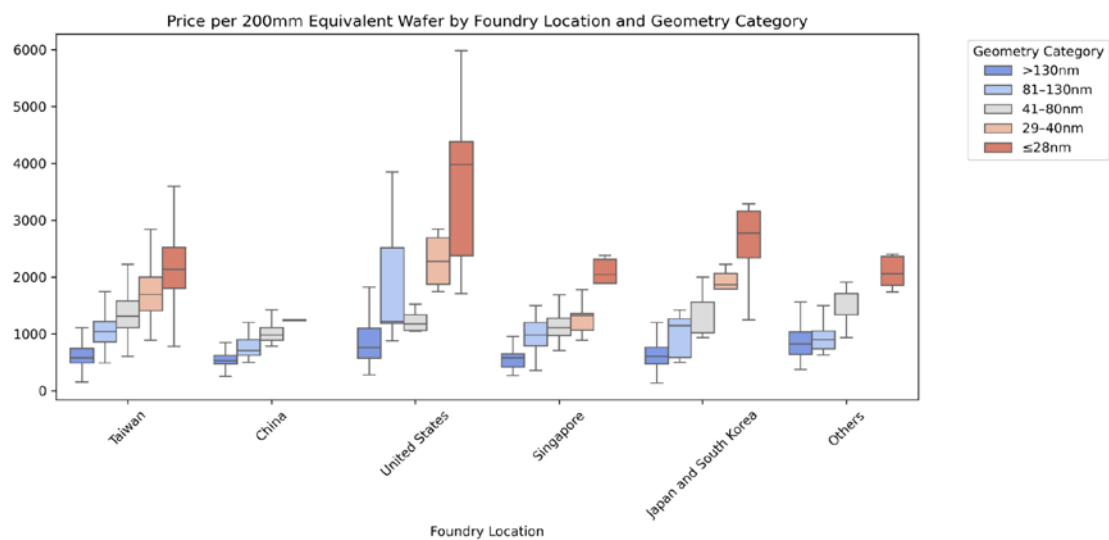


Figure 29: Semiconductor Wafer Prices by Foundry Location



**Table 3: Regression of Log Price per Wafer on Product Characteristics
(China, $\geq 350\text{nm}$, 2012 as base group)**

Dep. Variable:	log_equivprice	R-squared:	0.717
Model:	OLS	Adj. R-squared:	0.716
Method:	Least Squares	F-statistic:	583.6
Date:	Sun, 27 Apr 2025	Prob (F-statistic):	0.00
Time:	22:43:14	Log-Likelihood:	-1301.7
No. Observations:	6493	AIC:	2679.
Df Residuals:	6455	BIC:	2937.
Df Model:	37		
Covariance Type:	HC3		

	coef	std err	z	Pz	[0.025	0.975]
Europe	0.4801	0.027	17.540	0.000	0.426	0.534
Japan	0.1352	0.049	2.739	0.006	0.038	0.232
Malaysia	0.2585	0.033	7.819	0.000	0.194	0.323
Singapore	0.0627	0.015	4.194	0.000	0.033	0.092
South Korea	0.2391	0.021	11.550	0.000	0.199	0.280
Taiwan	0.1120	0.011	10.228	0.000	0.091	0.133
United States	0.4795	0.019	25.061	0.000	0.442	0.517
181–350 nm	0.1900	0.033	5.813	0.000	0.126	0.254
131–180 nm	0.2702	0.035	7.632	0.000	0.201	0.340
81–130 nm	0.4804	0.037	12.944	0.000	0.408	0.553
41–80 nm	0.7048	0.040	17.433	0.000	0.626	0.784
29–40 nm	0.8927	0.043	20.557	0.000	0.808	0.978
28nm	1.0466	0.046	22.823	0.000	0.957	1.136
2013	-0.0665	0.013	-5.028	0.000	-0.092	-0.041
2014	-0.1014	0.014	-7.106	0.000	-0.129	-0.073
2015	-0.1007	0.016	-6.273	0.000	-0.132	-0.069
2016	-0.1270	0.017	-7.469	0.000	-0.160	-0.094
2017	-0.1129	0.018	-6.381	0.000	-0.148	-0.078
2018	-0.1437	0.017	-8.213	0.000	-0.178	-0.109
2019	-0.1718	0.018	-9.308	0.000	-0.208	-0.136
2020	-0.2049	0.018	-11.467	0.000	-0.240	-0.170
2021	-0.1303	0.020	-6.642	0.000	-0.169	-0.092
# Metal Layers	0.0392	0.004	9.424	0.000	0.031	0.047
# Poly Layers	0.0515	0.009	5.447	0.000	0.033	0.070
log # wafers	-0.0488	0.006	-8.130	0.000	-0.061	-0.037
# Process Masks	0.0194	0.001	18.406	0.000	0.017	0.021

Notes: Standard Errors are heteroscedasticity robust (HC3). Controlling also for wafer size, size of order FEs.

Fact 6: Capacity, Investment Ramp Up From: Government Investment

To test whether government equity injections impact firms' equipment investment and capacity increases, I estimate event study regressions of the following form

$$y_{it} = \sum_{k=-40}^{40} \beta_k \mathbb{1}(\text{first-time GF investment at quarter } t-k)_{it} + \gamma' X_{it} + \delta_i + \rho_t + \epsilon_{it} \quad (3)$$

with y_{it} being outcomes of interest such as log 200mm equivalent capacity, log equipment investment, log(capacity/capital), and process node (geometry) of the plant i at quarter t . X_{it} are plant age and log registered capital, δ_i and ρ_t are the plant and quarter fixed effects, and standard errors are clustered at the firm level as before. Plots of coefficients from Figures 30 and 31 suggest that plant capacity and equipment investment increased markedly after a government guidance fund investment event, suggesting that government equity injections could substantially relax capital constraints of these firms. As capacity and capital investment both increase, figure 32 shows the event study regression with log (capacity/capital) as outcome. The coefficient estimates are largely imprecise, but we see that after an initial small dip in capacity productivity, plants slightly improve their capacity/capital stock ratio. This suggests that in addition to capital support, on average there are some improvements in capital utilization and management practices after government investment. This could be an

outcome of guidance fund managers entering the firm's board after acquisition of a substantial stake, or that local governments offering additional infrastructure and other intangible support along with equity injections. Innovations in technology process node, wafer size, and the number of layers (in case of 3D NAND memory) are other measures of firm performance. I summarize these events by an indicator measure for each quarter $\times$ firm if the firm achieves the following: (1) innovating in the process node (either within one of its existing plant or building a new plant with a more advanced node than what the firm was currently producing), (2) innovating in wafer size by increasing the size of wafers, or (3) increasing the layers of its memory product in any preexisting plant or a new plant. I then regress this indicator measure on indicators of leads and lags of the guidance fund investment event with firm and quarter FEs. Figure 33 plots the event study coefficients with fully saturated leads and lags. It is apparent that barring a few spikes, portfolio firms of government guidance

funds do not in particular achieve significantly more progress in the aforementioned product technology dimensions after a government investment event. These results are consistent with local government objectives that largely target total output and sales rather than innovation per se.

Figure 30: Equipment Investment Before and After Government Guidance Fund Investment Event

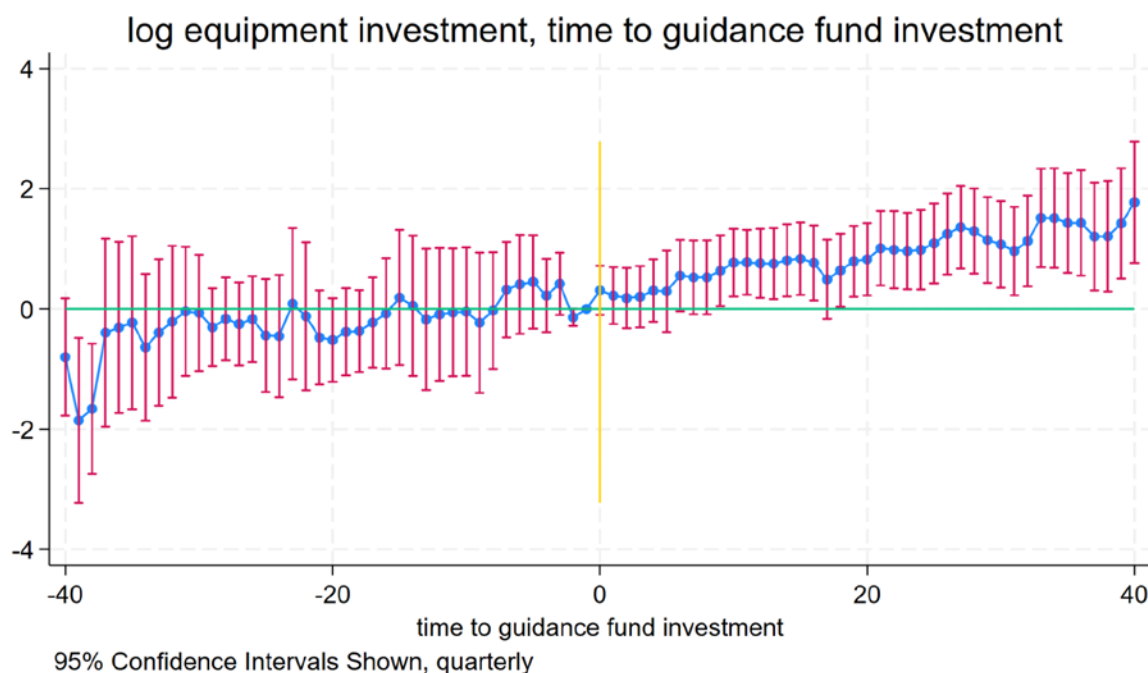


Figure 31: Log 200mm Equivalent Capacity Before and After Government Guidance Fund Investment Event

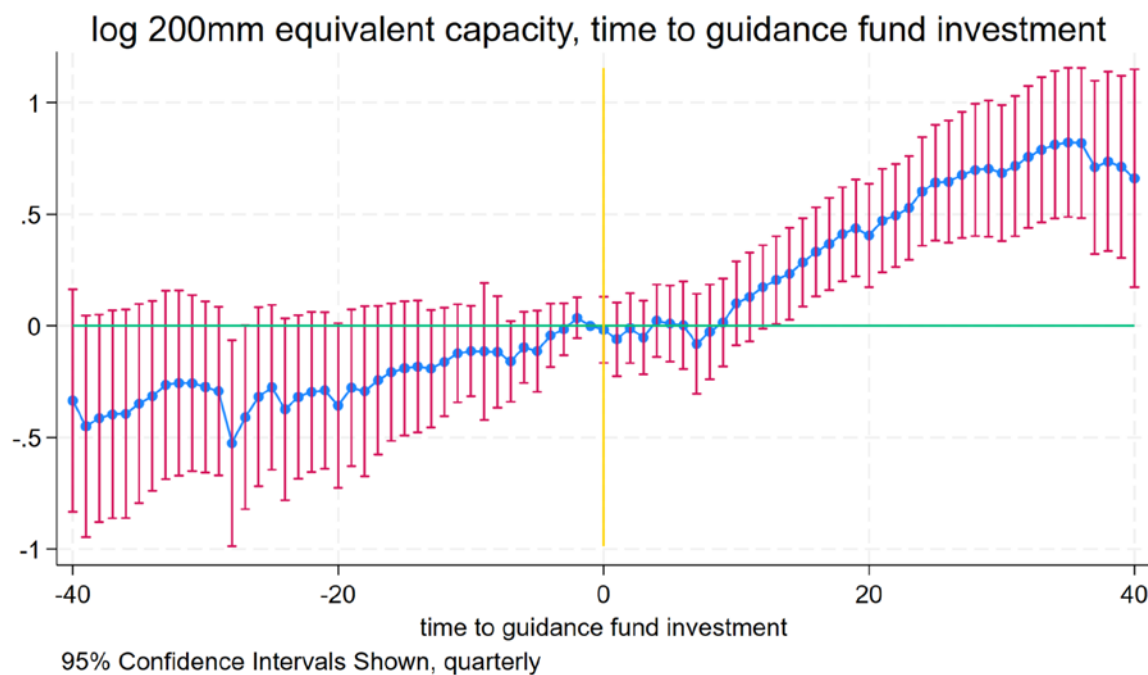


Figure 32: Log (Capacity/Capital) Before and After Government Guidance Fund Investment Event

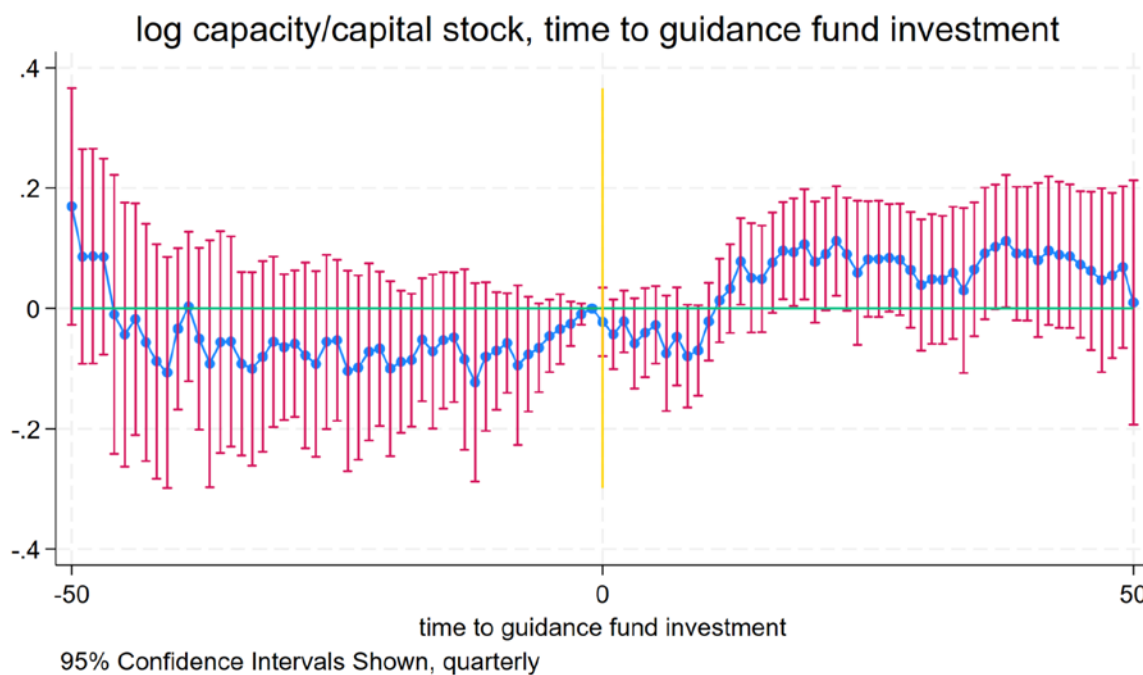
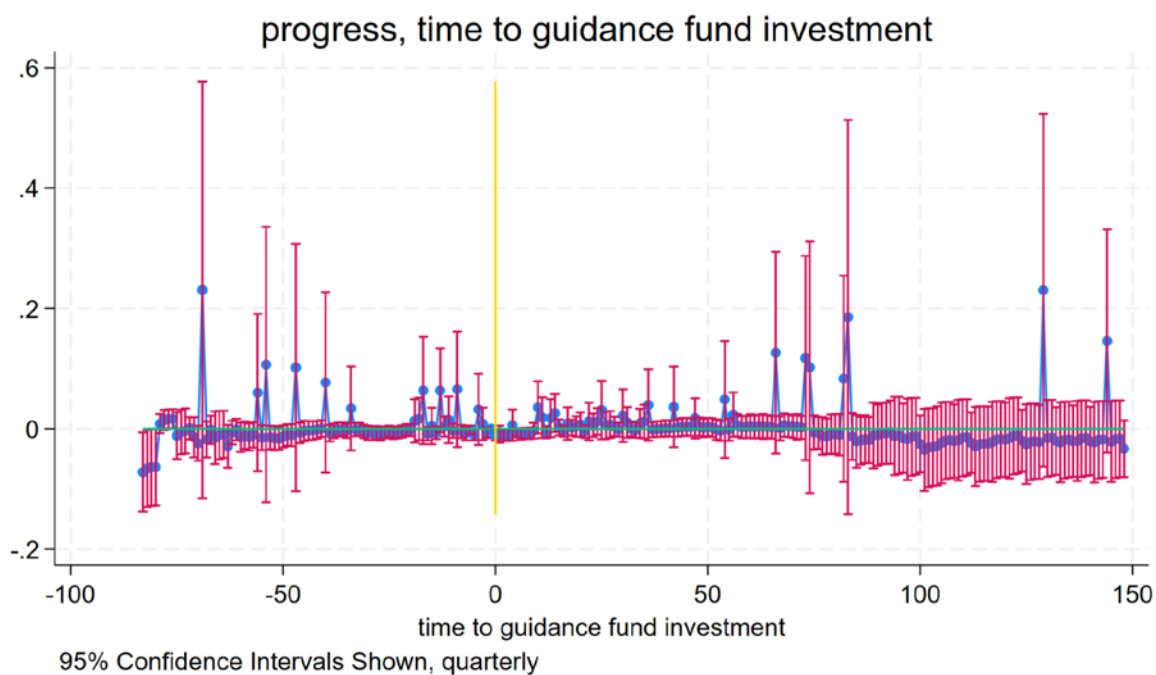


Figure 33: Plant Process Node Innovation Before and After Government Guidance Fund Investment Event



Figures 34, 35, and 36 plots the most advanced technology process node of leading foundries. memory, and analog/discrete firms. in China from 2013-2024. Figure 37 plots the number of 3D layers of NAND firms. The color of the squares represents the foundry's ownership status. For leading semiconductor domestic firms in China, the variation in ownership status through time reinforces with the empirical Fact 3 documented above. Local government funds play a key role in incubating fledgling manufacturers such as NexChip and CXMT in Hefei, United Nova in Shaoxing, and Si'En in Qingdao. They also supported costly and risky process node upgrading of growing firms such as HLMC, Silan, and GTA Semiconductor (ex-ASMC) before the central government funds chip in. A cursory examination of the time series across companies suggest that local and central government investment generally coincides and precedes that of significant and continuous progress in process node. Yet a potential reason why such data did not get reflected in the regression coefficients of Figure 33 is that non-invested companies, in particular foreign firms such as TSMC, UMC, Texas Instruments, SK Hynix, and Samsung, also accelerated process node innovation of their facilities within China at a significant pace. This is likely a reaction to competitive pressures from Chinese progress and growing market opportunities.

Finally, I study whether there is variation in productivity effects between local and central government guidance fund investments, given results in Fact 3 that local portfolio firms are more productive than their local peers but the central portfolio firms are not particularly productive nationally. Figures 38 and 39 show the event study coefficients of local and central government fund investment events

with the national z-score of capacity/capital as outcomes. It is striking that after a local government guidance fund investment event, local government champions gradually improve their national productivity ranking within their sector. This corresponds to the narrative that local government champions gradually grew to become nationally competitive champions years after the investment event. Little productivity effect is observed for central government investment, which in combination with the fact that central government investments trail that of the local government suggest that local government investments have been an important driver of productivity improvements and capacity expansion in Chinese semiconductors.

Figure 34: Most Advanced Node and Ownership Status by Time, Logic Foundries

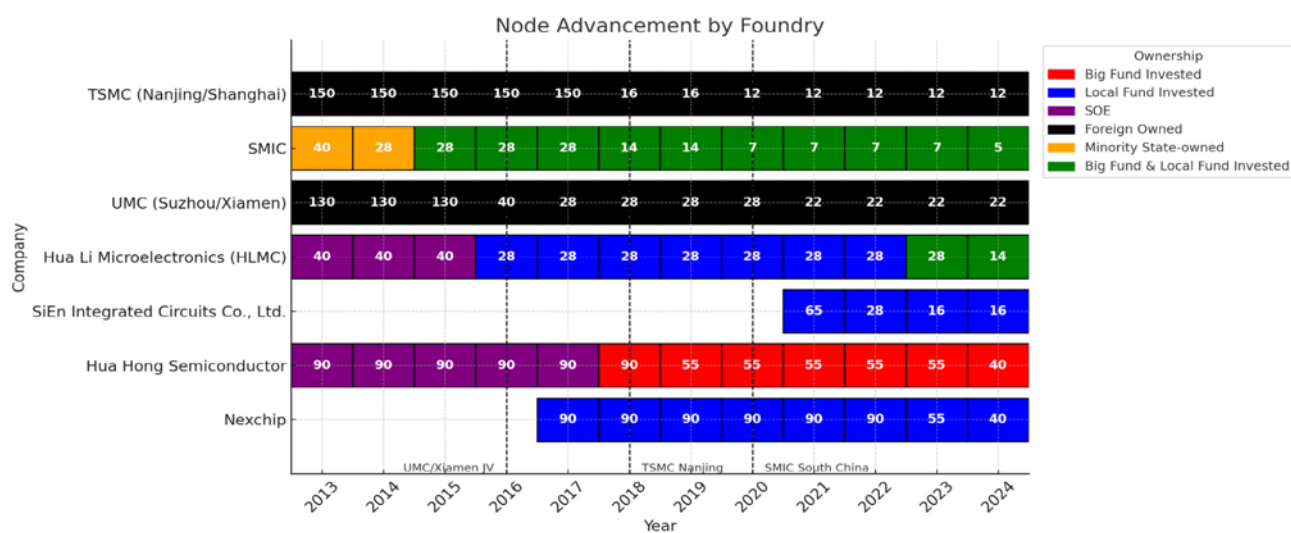


Figure 35: Most Advanced Node and Ownership Status by Time, Memory Firms

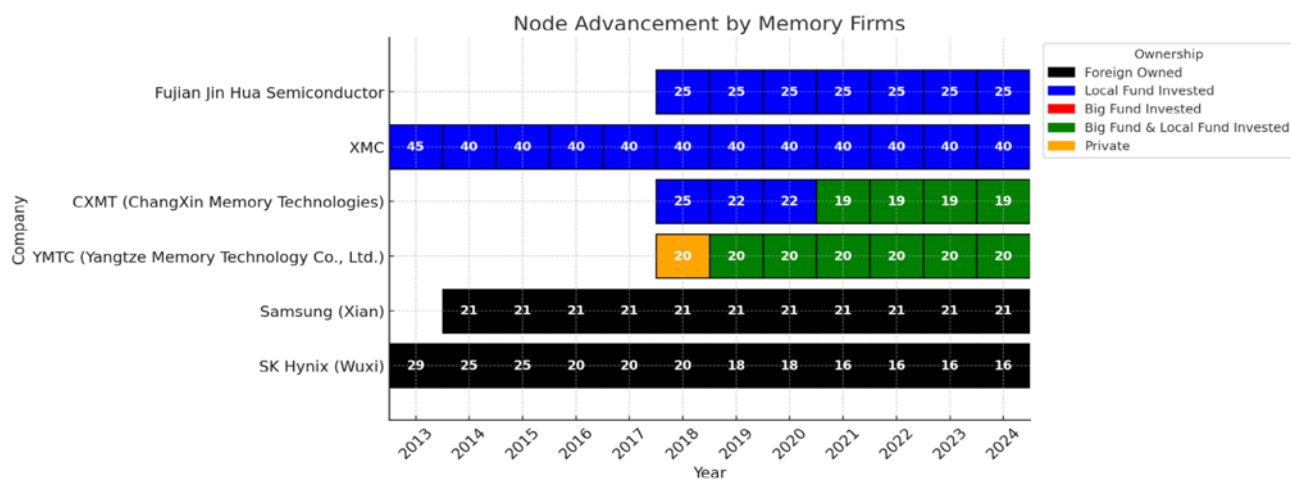


Figure 36: Most Advanced Node and Ownership Status by Time, Discrete/Analog Firms

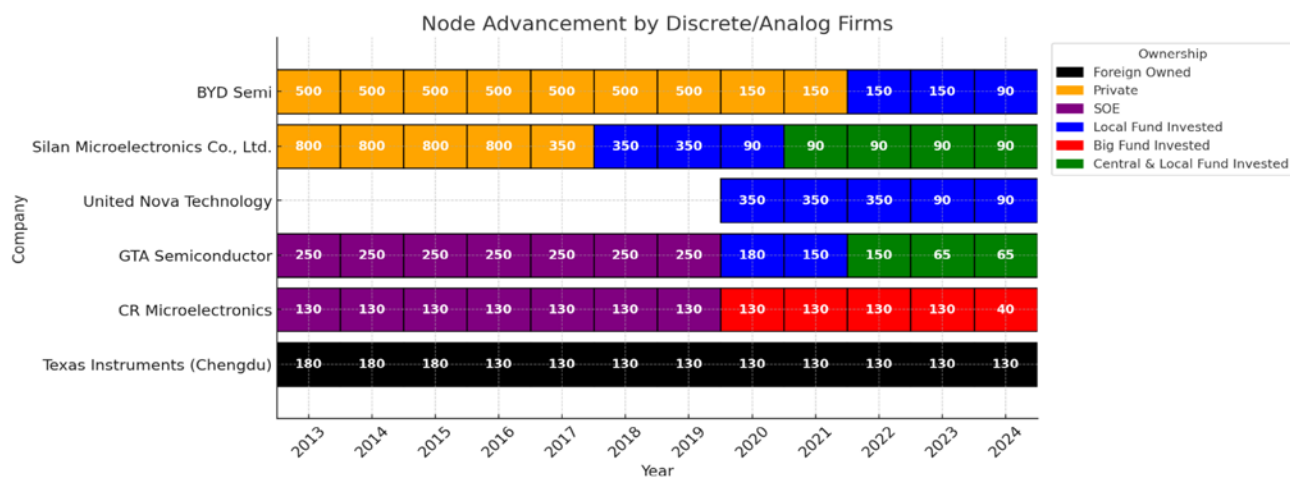


Figure 37: Max Layers Produced, 3D NAND Firms

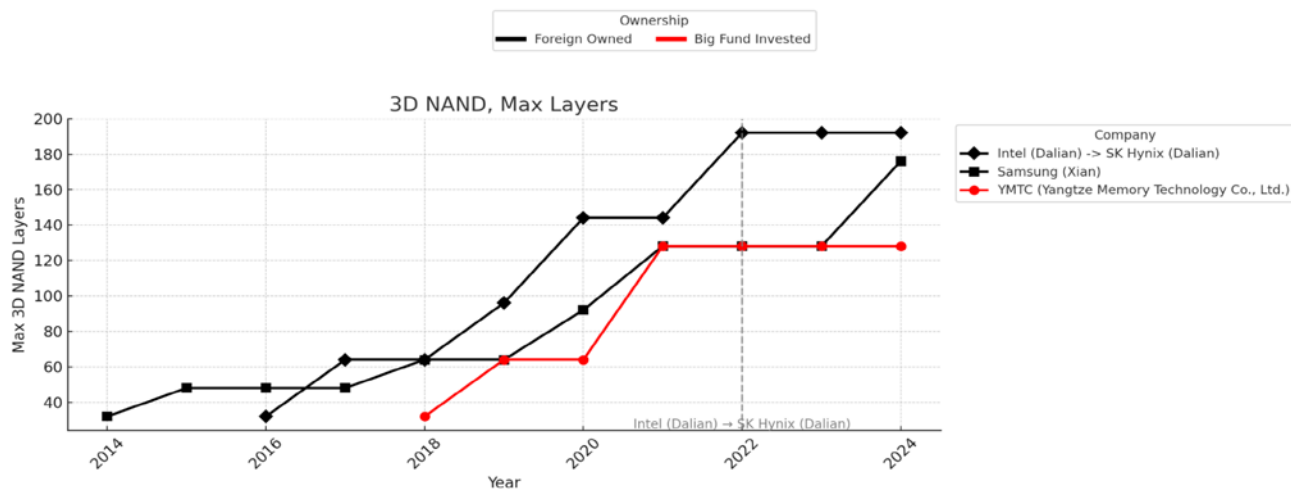


Figure 38: National Capacity/Capital Z-Score Before and After Local Government Guidance Fund Investment Event

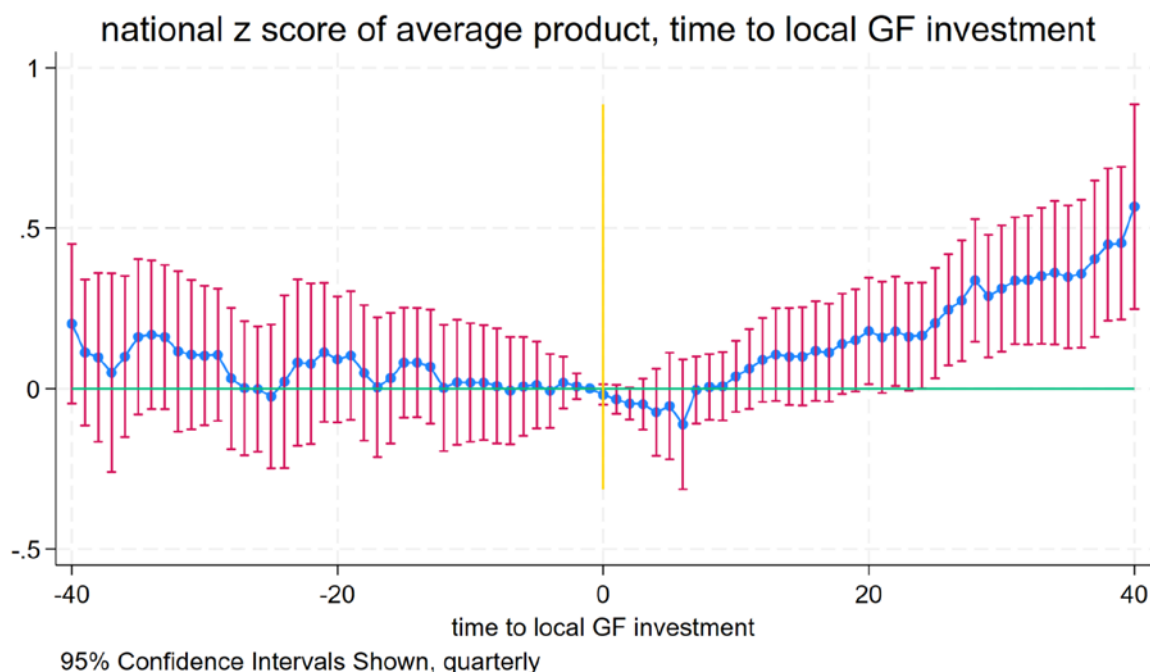
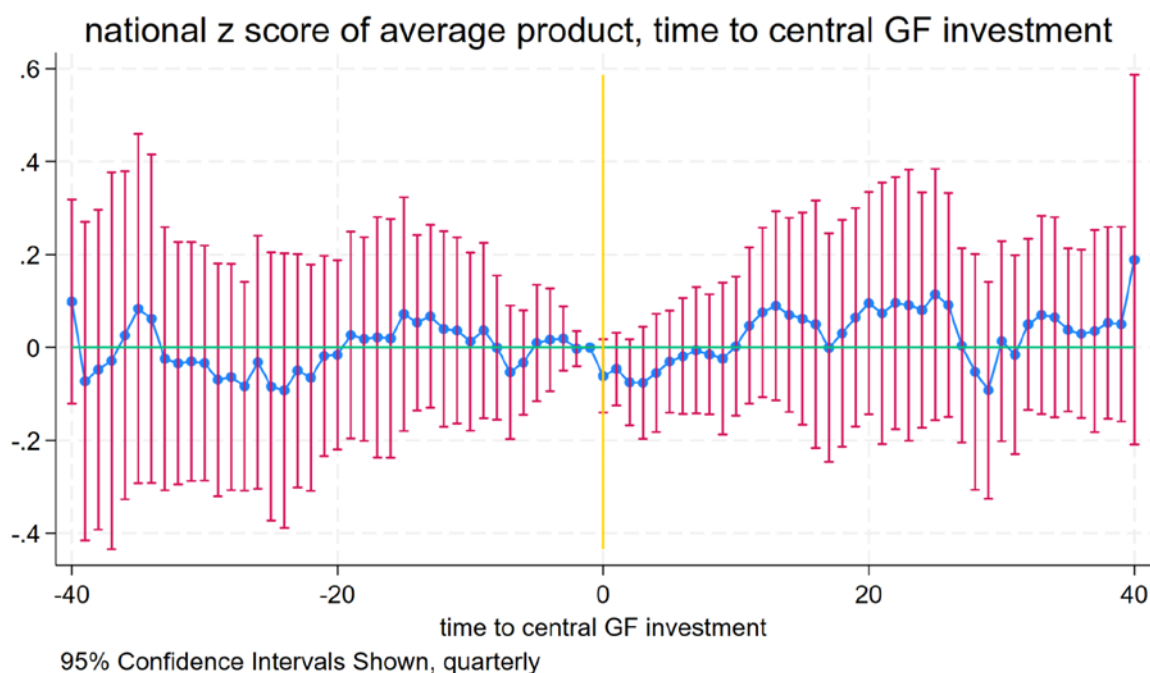


Figure 39: National Capacity/Capital Z-Score Before and After Central Government Guidance Fund Investment Event



Conclusion

Decentralized Drive, Centralized Ambitions

With the rise of Chinese market shares in compound semiconductors, memory, and mature logic chips, the apparent wastefulness and inefficiencies of Chinese semiconductor industrial policy touted in media are now being revisited. Apart from notorious failures like [Wuhan Hongxin⁷⁴](#), local governments have nurtured champions threatening to be globally competitive in various subsectors: Hefei's [CXMT⁷⁵](#) is now rapidly catching up with leading memory producers in DRAM and high-bandwidth memory (HBM) vital for AI applications, Wuhan's [YMT⁷⁶](#) is now at the global technological frontier in NAND Flash (hard drive), while Shenzhen, apart from supporting various fab projects in memory and legacy logic affiliated to [Huawei⁷⁷](#), backed [SiCarrier⁷⁸](#), which recently announced breakthroughs that have apparently made it the most capable Chinese champion in semiconductor manufacturing equipment.

Similar to the origins of well-known national champions like SMIC and Huawei, a common theme linking these younger rising Chinese firms is that they started off as nascent projects heavily supported by local governments that grew to be nationally and internationally competitive. Thus understanding the dynamic political economy incentives driving local government industrial policies is vital to arrive at a full picture of the development of the Chinese semiconductor industry. Western commentaries typically gloss over this decentralized facet of Chinese semiconductor efforts, and often make analyses that assume the Chinese state to be a

unitary actor aiming towards national self-sufficiency. The reality is that industrial policies are executed by multiple actors with conflicting objectives. The central government wishes to coordinate national resources yet exploit local flexibility to create competitive national champions across the supply chain nationally. Local governments instead are determined to nurture a fully local domestic supply chain from chip design, manufacturing, to final consumer products that is superior to that of other localities. As a result, despite unprecedented government support towards the sector nationwide, the support is diffused across firms residing in different localities within each subsector. Scattered support results in subsidy misallocation as many unproductive firms survive off misguided government subsidies, yet another consequence is that market competition forces are preserved. True entrepreneurs are incentivized to continue to innovate and cut down costs as prices decline. In this process, incapable or fraudulent projects drop out of the market over time, while capable local champions rise to gain market share and national attention, ultimately becoming national champions supported by the central government.

These distinguishing features of Chinese decentralized industrial policy explain several puzzles of the development of the Chinese semiconductor industry: the relentless rise of Chinese semiconductor manufacturing capacity especially in the mature technologies, the presence of multiple state-supported producers in the same sector that continue to produce and build despite declining prices, simultaneous support across firms on the supply chain, and the emergence of globally competitive firms

supported by local governments despite similarly spectacular failures early on. Proper understanding of the fundamental decentralized institutions of Chinese industrial policy is necessary for other Western and East Asian economies to mount the correct response to emerging Chinese technological and production capabilities. Attributing Chinese capacity expansion as deliberate intent by the Chinese central state to “flood” global markets with excess production is misguided as capacity expansions are driven by numerous competing firms including both leading national foundries SMIC and Huahong as well as local manufacturers supported by provincial/city governments. In fact, official central government rhetoric and comments by national champions such as [SMIC](#)⁷⁹ have repeatedly warned against mature node overcapacity that could lead to unsustainable price wars.

Central policies have been encouraging consolidation and price coordination across all advanced manufacturing sectors that have witnessed the same phenomenon, such as [solar panels](#)⁸⁰, [EVs](#)⁸¹, and [semiconductors](#)⁸². The adamant focus of local government policies on meeting output/sales and national market share targets without reference to industrial profits is instead the primary driving force of Chinese manufacturing capacity. This may not be ideal from the central government’s perspective if it wishes to concentrate resources on the most productive and competitive firms nationally, which explains recent efforts by the central government to industrial policy efforts by delegating Huawei to organize a [vertically integrated domestic supply chain](#)⁸³ of national champions while [reducing local government participation in the 3rd phase of the Big Fund](#)⁸⁴,

keeping only equity participation from Beijing, Shanghai, and Guangdong. In the critical equipment industry, apparently now the government is also directing efforts to [consolidate](#)⁸⁵ about 200 toolmakers nationwide into 10. Whether centralization of resources would bring the scale benefits as common wisdom suggests remains to be seen. Decentralization has brought staggering loss of resources to misallocation, but to rely on the central authority making the right decisions in each niche subsector across the complex hardware supply chain is equally difficult. How to maintain the incentives of competition and benefits of nimble local experimentation under the new centralized regime remains a daunting task for China.

Policy Recommendation

For policymakers around the world interested in mitigating the impact of Chinese production on their respective mature node producers’ business outlook, denying exports of inputs such as manufacturing equipment and materials applicable to more mature nodes could create short to medium term disruption as China still generally lacks market share in home-grown equipment and material solutions in the 14-65 nanometer range. Yet as Chinese firms have successfully developed domestic solutions, a blanket ban would create room for Chinese alternatives, enabling high production costs to reduce overtime from learning by doing. As mature Chinese manufacturing equipment and materials take up close to half of the revenue of US and aligned countries’ suppliers, the resistance to such measures will be immense from the industry and other governments. The

cost calculus thus is not obvious from the US government's perspective, as a multilateral export control regime is less likely now with the current administration's preference for unilateralism and actions that have alienated European and East Asian allies.

Similar arguments could be applied to EDAs, on which Washington has very recently implemented an apparent universal [export control](#)⁸⁶ of products by Synopsys, Cadence, and Siemens EDA to Chinese firms via a licensing regime. Unlike equipment and materials, market concentration of US-based firms in EDAs allowed the US Department of Commerce to weaponize EDA control unilaterally. A blanket ban of EDAs could severely affect Chinese designers' access to Taiwanese, Korean, and Western foundries both inside and outside of China, especially to processes between 3 and 28 nanometers where full-stack Chinese EDA commercial solutions are lacking. For designers such as Huawei HiSilicon and Cambricon, the EDA restriction is likely to be less effective as they are probably either using homegrown solutions or alternative sources for license via pirating or third-parties. However, EDA export control could hurt nonrestricted designers that are competing with Huawei, such as Xiaomi which had recently announced a 3nm mobile chip fabbed at TSMC.

Regarding >28nm mature nodes where China is in principle self-sufficient from software, materials, equipment, and to manufacturing, the US and aligned countries will likely resort to strategic trade policies that encompass tariffs, outbound investment controls, and even direct import bans for certain end uses. Yet unilateral tariff regimes that singularly target China may

be not totally effective in restraining Chinese mature node advances or protect domestic mature chipmakers for two reasons: first, Chinese manufacturers are competing with other countries' mature chipmakers for customers within China and other countries, as Chinese domestic self-sufficiency remains low even in mature node semiconductors⁸⁷. Second, even if a country faces dumping of semiconductors from China, imported Chinese chips are likely to be embedded in electronic components that get shipped across multiple borders, making it impossible for customs to determine its origin in a reasonable component tariff regime. This is especially so when importers have strong incentives to mark down the percentage of value produced in China. Taxing end use consumer products involving components from China is likely to be politically unpopular in many countries. Rerouting of goods and relabeling of country of origin across the supply chain also make taxing semiconductor downstream products impractical without further collaboration among key nations on the supply chain on a standard to track shipments and determine country of origin of components. Taiwan stands as a crucial nexus in the supply chain due to its unique cost advantage in electronic assemblies and foundry production.

The US, Europe, and Like-minded East Asian countries like Taiwan and South Korea should therefore negotiate a joint sectoral agreement to determine joint tariffs and outbound investment restrictions, establish within-bloc free trade across the supply chain, and coordinate on capacity and specialized process R&D. As the United States is implementing unilateral tariffs via a Section 301 investigation on Chinese mature semiconductors and another

Section 232 on the semiconductor, semiconductor equipment, and derivative products sector while instituting investment guardrails on China, European IDMs are [doubling down](#)⁸⁸ on joint ventures and supply agreements with Chinese firms, which are contrary to the Americans' intentions to counter Chinese overcapacity. This highlights the need for a multilateral regime to jointly coordinate on outbound investment and tariff policies. A necessary precondition for such a multilateral regime would be commitments to zero tariffs and free trade of semiconductor manufacturing inputs and derivative products, to allow each firm within the bloc to exploit its natural comparative advantage to counter Chinese nonmarket actions at the lowest possible cost. Furthermore, the multilateral regime serves as a platform to consolidate production and integrate the expertise of American, European, Taiwanese, and Korean foundries to not fall into spiraling price wars with each other and Chinese producers. Policies to ensure sufficient within-bloc demand for allied country producers' products are also crucial. Trusted Foundry programs that preferentially award contracts of strategic military, telecommunications, and space applications to selected firms could also ensure market demand and innovation.

Promotion policies that target R&D of specialized niche processes that enable mature node producers to differentiate themselves in the intricate mature logic and analog market should be prioritized. Subsidies from the US, Japan, and Europe towards automotive and compound semiconductor production capacity are likely to backfire and be inefficient as they serve only to aggravate the overcapacity issue. This is evidenced by [delays and downsizing](#)⁸⁹ of TSMC's

Kumamoto fab and the imminent bankruptcy of major US SiC supplier [Wolfspeed](#),⁹⁰ a grantee of the CHIPS Act. The Chinese central government's efforts towards consolidation and vertical integration shed light on how non-Chinese firms and governments could properly respond accounting for market realities. Strategic collaboration between Intel and Taiwan's UMC on a 12nm process that combines Intel's advanced facilities in the US and UMC's foundry business expertise is exemplary of how allied nations' foundries could join forces for their business advantage. Other touted consolidation measures include a rumored GlobalFoundries merger proposal with UMC that seems unlikely to materialize, yet it does suggest potential synergies from strategic partnership or collaboration between US and Taiwanese firms. Managed capacity planning and joint R&D between non-Chinese firms, in combination with restrictions on Chinese imports and promotion policies targeting specialized processes, will be critical for the US and its allies to withstand the China semiconductor challenge.

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