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Economic Security Program

The Great Breakout: Advanced Packaging and China's Race for AI Compute Parity

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About DSET

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Executive Summary

Moore's Law is no longer the semiconductor industry's sole organizing principle. As transistor miniaturization approaches its physical and economic limits, chip manufacturers are increasingly turning to advanced packaging to drive the next wave of semiconductor innovation. This shift has profound consequences for the U.S.-China technological rivalry. Advanced packaging has become China's primary vehicle for working around U.S. export controls on advanced-node semiconductors, allowing Chinese firms to achieve AI compute performance competitive with leading American chips without requiring access to leading-edge process nodes.

The current export control regime is designed around a node-centric logic—restricting China's access to advanced fabrication equipment, EDA tools, and high-end AI chips. That logic is insufficient. As this report's supply chain analysis demonstrates, the most important regulatory gap lies not at the front end of the semiconductor supply chain, but at the back end: in the upstream materials, manufacturing processes, and system-integration capabilities that underpin advanced packaging. China remains dependent on foreign suppliers for many of the materials and process capabilities that advanced packaging requires, yet these inputs remain almost entirely outside the reach of U.S. export controls.

This report recommends a systematic extension of export controls to the advanced packaging supply chain, targeting the materials, manufacturing technologies, and system-integration capabilities that current controls leave unaddressed. Taken together, these measures would raise the engineering integration costs and structural friction along China's advanced packaging circumvention pathway and restore meaningful leverage to an export control regime that is currently being outpaced.

Key Findings

- **Node-centric export controls have created a structural blind spot that China is actively exploiting through advanced packaging.** Since 2018, U.S. export control policy has scaled its restrictions in proportion to a semiconductor's process node. However, Chinese firms, most prominently Huawei, are leveraging advanced packaging to integrate multiple dies into multi-chip systems, achieving system-level AI compute performance that is projected to approach or even exceed export control thresholds despite sustained constraints on access to leading-edge fabrication.
- **Advanced packaging has restructured the semiconductor value chain, dissolving the traditional division of labor between foundries, OSATs, and system integrators.** As heterogeneous integration has matured, a distinct middle-end of line process has emerged as the principal battleground for signal efficiency, interconnect density, and power management. Foundries are pushing downstream into packaging; OSATs are building proprietary upstream capabilities. The result is a supply chain in which critical chokepoints are distributed across multiple tiers of the value chain.
- **The current export control regime contains its most consequential regulatory gap at the upstream materials and OSAT tiers of the advanced packaging supply chain.** Controls are concentrated at the chip performance threshold and semiconductor manufacturing equipment tier, leaving upstream materials (ABF film, BT resin, and specialty glass

fabric) and OSAT-level packaging processes almost entirely outside the reach of the Export Administration Regulations. China cannot domestically produce these inputs at the specifications required for AI and HPC packaging applications, yet they remain outside the scope of export controls.

- **China has constructed a layered institutional architecture that converts advanced packaging from a technical possibility into operational compute capability.** China has absorbed the yield uncertainty, capital risk, and long payback periods that would otherwise deter private investment through the Big Fund, state-directed "demand-side lock-in," and local government-led national champion selection. This whole-of-nation mobilization has accelerated China's advanced packaging ecosystem from the policy margins to the core of its AI development agenda, allowing firms to iteratively improve packaging yields and capabilities.
- **China's advanced packaging strategy prioritizes system-level performance over node-level parity.** Rather than competing head-on with the United States at the leading edge, China is leveraging its substantial industrial base in mature nodes, OSAT capacity, substrate manufacturing, and fan-out panel-level packaging to achieve deployable compute performance for AI training and inference workloads.
- **Huawei's Ascend series demonstrates that system-level compute performance can improve across successive generations even under sustained process-node restrictions.** The Ascend 910C already achieves roughly 60 percent of NVIDIA H100 inference performance through multi-die integration and advanced packaging rather than process-node advancement. Successive generations are approaching performance levels that U.S. export controls were designed to prevent China from reaching. While export controls have constrained the ceiling of chip-level performance, system-level compute capability continues to expand, effectively raising the floor of deployable AI compute in China.

Recommendations

- **Extend export controls systematically to the advanced packaging supply chain.** The current control regime is built around front-end fabrication and chip performance thresholds. It leaves upstream materials, OSAT-level packaging processes, and system-level integration largely unaddressed. Controls should be expanded across four complementary dimensions: materials, technologies, products, and anti-circumvention enforcement.
- **Establish specification-based controls on concentrated upstream materials, prioritizing a U.S.-Japan minilateral framework.** ABF film, BT resin, specialty glass fabric, and high-end bonding materials constitute chokepoints where China has not achieved indigenous substitution capability and where supply is heavily concentrated among Japanese suppliers. Rather than imposing blanket export bans, controls should be calibrated to technical threshold parameters to restrict only the specifications required for AI and HPC packaging applications.
- **Impose quantitative threshold-based controls on advanced packaging manufacturing technologies and associated equipment.** Hybrid bonding, 2.5D and 3D heterogeneous integration, high-density substrate fabrication, and fine-pitch micro-bump processes are the core manufacturing capabilities enabling China's system-level circumvention strategy. Controls should be defined by explicit technical parameters rather than broad designations of

"advanced packaging technology," to ensure precision and enforceability. Because relevant equipment suppliers span Japan, the Netherlands, South Korea, and the United States, this pillar requires broader multilateral coordination than material-level controls.

- **Expand the control baseline from individual chip specifications to system-level performance after packaging integration.** Current controls permit sub-threshold chips to be integrated through advanced packaging into systems that surpass controlled performance levels. Product specification controls should cover finished substrates, packaged AI and HPC modules, and high-bandwidth memory, supported by end-user certification requirements that trace controlled products to their final installation location and application.
- **Construct a systematic anti-circumvention architecture to close enforcement gaps in Southeast Asia and other transshipment-risk regions.** Self-reporting by individual firms is insufficient to prevent diversion through third-country transshipment, end-use misrepresentation, and supply chain intermediaries. The United States and its allies and partners should establish mandatory disclosure obligations, anomalous order screening, transshipment verification, and a minilateral information-sharing framework to prevent regulatory arbitrage across jurisdictions.

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1.1 From Moore’s Law to “More than Moore”: Why Advanced Packaging

As the world approaches the limits of Moore’s Law, chip manufacturers are shifting innovation from front-end transistor scaling to back-end system production. To overcome both the physical and economic constraints of transistor miniaturization, manufacturers are increasingly relying on advanced packaging.[1] Advanced packaging builds upon traditional semiconductor packaging by interconnecting and stacking multiple small chips (or “chiplets”) to improve the performance, energy efficiency, and interconnect density of integrated circuits (ICs).[2]

Advanced packaging has restructured the semiconductor value chain. What was once a downstream afterthought—the assembly and packaging of already-fabricated chips—has become as consequential as chip design and fabrication. Mastery over advanced packaging processes now shapes system-level performance outcomes in the AI race, making it a source of strategic leverage rather than a back-end commodity.

Yet the United States has limited footing to exercise that leverage. During the era of globalization, America “off-shored” its industrial capacity; in the era of economic security, it seeks to “re-shore” the very capacity that has been lost. Since the 1990s, the United States’ semiconductor manufacturing base atrophied as firms shifted to a fabless-foundry model.[3] As a result, American firms outsourced not only the manufacturing of semiconductors, but also the assembly, testing, and packaging (ATP) of chips. The United States now holds a 3 percent share in global advanced packaging production, while most of it is concentrated in the Asia-Pacific.[4]

Advanced packaging has emerged as a critical battlefield in the U.S.-China technological rivalry. System-level integration and high-bandwidth, low-latency data transfer between logic and high bandwidth memory (HBM) are crucial for AI workloads, where memory access speed determines computational throughput—and it is precisely these capabilities that advanced packaging enables. This gives the People’s Republic of China (PRC, or China) a pathway to partially offset the performance constraints imposed by U.S. export controls on semiconductors crucial for AI computing. Against this backdrop, the United States and its allies and partners are moving to re-shore and “friend-shore” their advanced packaging capacity.

This chapter proceeds in three parts. It first traces the logic of *node-centrism* that has shaped U.S. export control policy since 2018, and how that logic has created a blind spot that China is actively exploiting through advanced packaging. It then surveys how the American policy community has framed advanced packaging as a dimension of economic security and the extent of legislative and executive branch action. Finally, it identifies two persistent policy challenges regarding node-centrism and the articulation of a coherent strategy that harmonizes both “promote” and “protect” tracks of economic security.

1.2 The Logic of Node-Centrism: From “The Great Siege” to “The Great Breakout”

Since the passage of the Export Control Reform Act of 2018, the United States has aimed to restrict the PRC’s access to advanced-node semiconductors.[5] While the United States has increasingly recognized the geostrategic importance of mature-node chips, current dual-use export control regulations (such as the Export Administration Regulations, or the "EAR")—enforced by the Commerce Department's Bureau of Industry and Security (BIS)—have yet to catch up, largely overlooking China's entrenchments into the foundational chip market.[6] Following a logic of node-centrism, American export control policy scales its restrictions in proportion to a semiconductor's generation, with controls tightening over cutting-edge "nodes."

For example, the first Trump administration primarily imposed export controls on entities, restricting their access to advanced chips for the development of dual-use technologies, as well as technologies used for surveilling ethnic minorities such as the Uyghurs.[7] The Biden administration broadened this approach, extending controls from semiconductor manufacturing equipment (SME) and software to advanced computing chips and their diffusion across third-country destinations.[8]

While American policy understandably prioritized restricting the flow of advanced chips to China, it neglected to address PRC's strides toward dominating the foundational chip supply chain. Just as China advanced a "Pseudo-IDM" strategy aimed at encircling and displacing the competitive advantage in foundational chips of the United States and its allies and partners,[9] China is now attempting to do the same with advanced packaging. To gain coercive leverage, China exploits policy blind spots. Chinese firms, such as Huawei, are circumventing U.S. export controls by stacking the best available domestic chips to achieve sufficient performance for large-scale deployment.

Advanced packaging is not merely a tool of Chinese circumvention, however. It is integral for maintaining a competitive edge in AI R&D, especially since AI relies on greater chip performance and efficiency. Leading American companies in AI such as Nvidia, Google, and AMD have secured the largest share of Taiwan Semiconductor Manufacturing Company's (TSMC) advanced packaging capacity, which currently leads the advanced packaging market with its chip-on-wafer-on-substrate (CoWoS) technology. This leaves mid-tier application-specific integrated circuit (ASIC) designers and other American chip manufacturers with inferior packaging alternatives.[10] As such, advanced packaging has become a focal point in American semiconductor policy.

1.3 American Semiconductor Policy and Advanced Packaging: Promote and Protect

American semiconductor policy operates along two tracks: promote, focusing on investment to re-shore critical industries,[11] and protect, utilizing export controls,[12] procurement restrictions, and allied coordination mechanisms to stymie technological gains made by adversarial nations. While the two are analytically distinct, they are strategically complementary, each serving the broader imperative of economic security.

1.3.1 Driving the Discourse: How Policy Research Has Presented Advanced Packaging

Policy research on advanced packaging has grown substantially in recent years, though it skews heavily toward the promote track. The Center for Security and Emerging Technology's John VerWey argues that re-shoring American advanced packaging capacity is critical for economic and national security. He notes that back-end production has become a "key determinant" in the development of emerging technologies.[13]

Similarly, Special Competitive Studies Project's Brady Helwig et al. telegraph the importance for American dominance in advanced packaging and heterogeneous integration.[14] They call upon the Department of Commerce and research and development (R&D) agencies to focus funds and efforts to propel the United States as the global leader of advanced packaging production by 2030.[15]

Where analysis has addressed the protect side at all, the prescription has often run in the opposite direction. Jack Whitney et al. from the Center for Strategic and International Studies acknowledge that Chinese firms evade U.S. export controls by "designing around" restrictions through advanced packaging methods. Instead of advocating for stricter export controls on advanced packaging technologies, they suggest doubling down on government efforts to expand American packaging growth.[16]

1.3.2 The Promote Track

Legislation

The landmark CHIPS and Science Act (known henceforth as the CHIPS Act) granted $39 billion in manufacturing incentives and $11 billion for R&D to revitalize America's domestic semiconductor ecosystem,[17] with Arizona designated as the hub for research and manufacturing.[18] Critically, the CHIPS Act allocated approximately $3 billion for the National Packaging Manufacturing Program (NAPMP), tasked with developing a "robust domestic advanced packaging ecosystem" through investment in packaging, equipment, and process innovation in partnership with research institutions including Arizona State University.[19] The CHIPS Act also established the National Advanced Packaging Piloting Facility (NAPPF) as the flagship physical R&D center for the NAPMP. The NAPPF equips researchers, startups, and firms with tools and resources to test and prototype advanced microchips in the United States.[20]

Testifying before the Senate Committee on Commerce, Science, and Transportation on the United States' advanced packaging capability, then-Commerce Secretary Gina Raimondo warned that the lack of domestic capacity to manufacture advanced packaging technologies posed a national security risk. She assured the committee that the Commerce Department would ensure the onshoring of multiple high-volume advanced packaging facilities by 2030.[21]

Congress has pursued complementary efforts to address specific packaging components. Influenced by the Global Electronics Association (formerly IPC), the Senate Armed Services Committee report on the FY 2025 Defense Appropriations Act directed the Department of Defense to brief Congress on initiatives to close industrial base gaps in electronics manufacturing. It included language on promoting a "silicon to systems" strategy, and the committee approved the allocation of $45 million for PCB manufacturing.[22] To address domestic production of specific components of advanced packaging systems, the Protecting Circuit Boards and Substrates Act ("PCB Act") was introduced in the House of Representatives in May 2025. If passed and signed into law, the bill would incentivize the domestic manufacturing of American-made advanced packaging systems by granting a 25 percent tax credit for firms that purchase American-manufactured PCBs and IC substrates.[23]

Executive Branch Action

President Biden's Executive Order 14017 on "America's Supply Chains" established the foundation for a subsequent Presidential Determination under Title III of the Defense Production Act (DPA) by linking a robust back-end ecosystem to U.S. military readiness and national security.[24] The determination formally designated PCBs and advanced packaging as essential to national defense. It waived certain funding requirements and authorized the Department of Defense to immediately utilize incentives for the domestic production of PCBs and advanced packaging.[25]

On the investment front, the current Trump administration secured what it has characterized as the "largest foreign direct investment in American history" from TSMC. Of the $100 billion announced in investments, some funds will be used for building two advanced packaging plants in Arizona.[26]

1.3.3 The Protect Track

Legislation

Allied coordination efforts have sought to extend the reach of American export controls through partner engagement. Introduced in the Senate in May 2024, the Coordinating AUKUS Engagement with Japan Act would require the Departments of State and Defense to assess Japan's export control system and identify areas in need of reform as a precondition for Pillar Two participation, specifically evaluating Japan's implementation of export controls on SME vis-a-vis China.[27]

Introduced in the House in September 2025, the China Advanced Technology Monitoring Act would require annual reporting on China's semiconductor manufacturing capabilities. The Secretary of Defense, in consultation with relevant agencies, would submit an annual report to both the House and Senate Armed Services Committees on China's production of advanced and mature node chips. The reports would include an assessment of China's development across the semiconductor value chain, to include: advanced packaging techniques, design, intellectual property (IP), R&D, industrial gases, silicon and critical minerals, and photomasks. They would also evaluate the effectiveness of American and allied export controls, including analysis of circumvention workarounds and third-party acquisition risks.[28]

On the procurement side, the Chip Equipment Quality, Usefulness, and Integrity Protection Act ("EQUIP Act"), introduced in the House and Senate in November and December 2025 respectively, would amend the FY2021 National Defense Authorization Act to prohibit recipients of government funding from procuring, installing, or using SME manufactured, assembled, or refurbished by a foreign entity of concern and designed for use in fabrication, assembly, testing, advanced packaging, or related R&D.[29]

Two significant pieces of pending legislation are the Semiconductor Technology Resilience, Integrity, and Defense Enhancement Act ("STRIDE Act") and the Multilateral Alignment of Technology Controls on Hardware Act ("MATCH Act").[30] The STRIDE Act was introduced in the House in November 2025 and advanced during a House Foreign Affairs Committee (HFAC) markup in late April 2026 amid a broader package of export control legislation.[31] The amended version would direct the Secretary of State to identify shared objectives with allies and partners on harmonizing export controls over SME, dual-use materials including photoresists, specialty gases, and advanced substrates, and emerging vectors of technology transfer including talent outflow, foreign direct investment (FDI), and espionage.[32]

Introduced with companion legislation in both chambers in April 2026 and amended during the HFAC markup,[33] the MATCH Act would complement the STRIDE Act by converting diplomatic objectives into binding legal obligations. Where STRIDE seeks allied coordination, MATCH would harden the BIS SME control regime. It would establish a statutory mandate, insulating export control policy from commercial or diplomatic pressure. The MATCH Act would expand the scope of SME destined for the PRC subject to presumption of denial controls, and it would impose a new licensing requirement for servicing applicable items at key semiconductor manufacturing facilities, limiting China's ability to maintain existing advanced tools after new sales are curtailed. It would also give allies 240 days to harmonize export controls. If the United States cannot certify full allied alignment, the Secretary of Commerce must impose unilateral export controls and extend U.S. jurisdiction to cover SME exported or reexported from non-compliant allied countries.[34]

Regulatory Updates

Since 2022, BIS export controls on advanced SME have concentrated mostly on front-end fabrication tools—a focus that has only recently begun to shift toward back-end processes. However, gaps remain. The October 2023 SME Interim Final Rule (IFR) codified this front-end orientation explicitly,[35] carving out back-end assembly, testing, and packaging activities from the end-use controls.[36]

This back-end exclusion is still valid today. In December 2024, BIS published an IFR on the Foreign Direct Product Rules ("FDP Rules") on advanced computing and semiconductor equipment. Specifically, this IFR contains two major "Direct Product" rules that bring certain foreign-made items under U.S. control if they are produced using U.S. technology or software:

> (1) **Footnote 5 FDP Rule:** This FDP Rule extends to specific entities on the Entity List (primarily those involved in PRC chip manufacturing). It restricts their ability to acquire foreign-produced SME that is the "direct product" of U.S. technology.
>
> (2) **SME FDP Rule:** This update expands export controls to advanced SME manufactured abroad using U.S. software or technology.[37]

Concurrently, BIS published a final rule adding 140 entities to the Entity List across China, Japan, South Korea, and Singapore, encompassing SME producers, materials companies, and precision equipment companies—bringing them within the scope of the Footnote 5 FDP Rule.[38]

Notably, the January 16, 2025 "Foundry Due Diligence" IFR brought outsourced semiconductor assembly and test (OSAT) providers into the compliance regime for the first time, requiring front-end foundries and OSAT companies to implement due diligence measures preventing the diversion of advanced ICs before they reach the intended end-user. BIS identified the packaging and testing stages as particularly vulnerable to export control circumvention.[39]

1.4 Challenges Ahead

Amid these developments, there are two primary challenges.

The first is node-centrism, the prevailing assumption that semiconductor capability maps neatly onto process-node advancement. This assumption generates two distinct vulnerabilities. Export controls focused on advanced nodes leave China's consolidation of the foundational chip market largely uncontested. Despite growing recognition of this risk, the United States has implemented no effective countermeasures. More fundamentally, node-centrism overlooks how advanced packaging and heterogeneous integration can generate meaningful system-level gains without frontier-node access, enabling China to partially compensate for chip performance restrictions through system architecture rather than process technology.

The second challenge is sustaining parallel momentum across the promote and protect tracks. These policy tracks are often treated as operating independently, but the legislative and executive actions taken since 2022 demonstrate that they can be mutually reinforcing (see Table 1.1). Promotion alone cannot offset China's industrial advantage in back-end manufacturing; protect policies are therefore indispensable while the United States rebuilds its domestic leverage.

The rest of the report is structured as follows. Chapter 2 establishes an analytical framework for advanced packaging as a strategic and regulatory object. It examines how advanced packaging has restructured the global semiconductor value chain, develops a three-pathway classification differentiated by technological capability, cost structure, and regulatory exposure, and maps the supply chain chokepoints where U.S. export controls hold and where they do not. It then traces the logic of China's asymmetric breakout strategy and the engineering constraints that bound it. Chapter 3 demonstrates how the PRC marshals national policy direction, state capital, and local competition to cultivate industry "national champions" and establish a domestic advanced packaging ecosystem. Chapter 4 provides a case study on Huawei's Ascend series of AI accelerators and examines how advanced packaging has enabled the company to iterate under export control pressure. Chapter 5 concludes the report and offers recommendations on how Taiwan, the United States, and other allies and partners can expand and enforce export controls across the advanced packaging supply chain.

Table 1.1. Protect and Promote: U.S. Semiconductor Policy vis-à-vis Advanced Packaging

Bills, Laws, and Actions	Type	Actors	Mechanism	Objectives
CHIPS Act (2022)	*Promote*	Congress; Commerce Department	NAPMP and NAPPF; TSMC investments in Arizona	The law aims to revitalize America's semiconductor manufacturing capacity.
DPA Title III (2023)	*Promote*	President; Defense Department	Defense Production Act Investment (DPAI)	The determination designates PCBs and advanced packaging as essential to national security and fast tracks domestic PCB and advanced packaging manufacturing.
FDP Rule Additions, and Refinements to Controls for Advanced Computing and Semiconductor Manufacturing Items (2024)	*Protect*	Commerce Department (BIS)	Interim Final Rule (IFR), 89 Fed. Reg. 96,812 (December 5)	The IFR extends export controls to foreign-produced SME involving listed entities and imposes new controls on HBM.
Additions and Modifications to the Entity List (2024)	*Protect*	Commerce Department (BIS)	Final Rule (Entity List Addition), 89 Fed. Reg. 96,830 (December 5)	The final rule adds 140 entities across China, Japan, South Korea, and Singapore to the Entity List. Controls encompass SME producers, materials companies, and precision equipment companies.

Bills, Laws, and Actions	Type	Actors	Mechanism	Objectives
Coordinating AUKUS Engagement with Japan Act (2024)	*Protect*	Congress; State Department; Defense Department	Allied coordination; export control assessment	The bill would direct the Departments of State and Defense to evaluate Japan's export control system, including SME controls toward China, as a precondition for AUKUS Pillar Two participation.
Implementation of Additional Due Diligence Measures for Advanced Computing Integrated Circuits (2025)	*Protect*	Commerce Department (BIS)	IFR, 90 Fed. Reg. 5,298 (January 16)	The IFR requires front-end foundries and OSAT providers to implement due diligence measures preventing IC diversion prior to reaching the intended end-user. Identifies packaging and testing stages as circumvention vulnerabilities.
Defense Appropriations Act (2025)	*Promote*	Congress; Defense Department; President	Discretionary funding	The act promotes a "silicon-to-systems" strategy in part by allocating $45 million for PCB manufacturing.
PCB Act (2025)	*Promote*	Congress; Commerce Department	Financial assistance program; 25% investment tax credit	The bill would incentivize domestic production of advanced packaging systems by granting tax credits for firms that buy American PCBs and IC substrates.
China Advanced Technology Monitoring Act (2025)	*Protect*	Congress; Defense Department	Congressional oversight; annual reporting	The bill would direct the Defense Department to monitor China's semiconductor manufacturing capabilities across the semiconductor value chain, including advanced packaging, materials, and industrial gases, and assess the effectiveness of U.S. and allied export controls.
Chip EQUIP Act (2025)	*Protect*	Congress; Commerce Department	Procurement restriction; funding conditionality	The bill would prohibit recipients of federal semiconductor funding from procuring, installing, or using fully assembled SME manufactured, assembled, or refurbished by a foreign entity of concern, including equipment used in advanced packaging and testing.
STRIDE Act (2026, as amended)	*Protect*	Congress; Secretary of State; Export Advisory Review Board	Allied coordination; FDPR; Entity List	The bill would direct the Secretary of State to identify shared objectives with allies on harmonizing export controls over semiconductor manufacturing equipment, dual-use materials including photoresists, specialty gases, and advanced substrates, and emerging vectors of technology transfer including talent outflow, FDI, and espionage. Where allied cooperation is insufficient, it would authorize remedial action under ECRA authorities.
MATCH Act (2026, as amended)	*Protect*	Congress; Commerce Department; State Department	EAR; FDPR	The bill would replace node-based specifications with a market dominance test, impose a universal license requirement with presumption of denial for servicing at key semiconductor manufacturing facilities, and give allies 240 days to harmonize export controls or face U.S. extraterritorial restrictions over their SME exports.

Source: Made by authors.

Chapter 2 | Shifting the Battlefield: From Front-End Nodes to Back-End Interconnects and Performance Pathways of Advanced Packaging

2.1 The Paradigm Shift: From Transistor Scaling to System Scaling

As Moore's Law reaches its physical and economic limits, advanced packaging has emerged as the industry's primary catalyst for capability gains. The law is no longer the industry's sole organizing principle, as exemplified by the Semiconductor Industry Association's decision to retire the International Technology Roadmap for Semiconductors and launch the Heterogeneous Integration Roadmap in 2015.[40] Advanced packaging innovates upon traditional packaging, which involves "protecting and connecting finished semiconductors," through the application of techniques and materials to increase the performance, energy efficiency, and interconnect density of ICs.[41] By partitioning large, expensive system-on-chips (SoCs) into smaller, functionally independent chiplets, these chiplets are then reassembled into a single package using 2.5D interposers or 3D stacking.[42] Just as urban planners build upward and outward when a city becomes more populated, chip designers stack and interconnect chips vertically and horizontally. This modular approach improves yield, shortens time-to-market, and decouples system performance from dependence on any single process node. Indeed, the industry has entered the era of "system scaling."[43]

While advanced packaging had mainly been used in consumer goods, such as mobile devices, it now plays an indispensable role in AI development. The explosion of generative AI, and large language models (LLMs) in particular, has exposed the limits of single-chip architectures. The binding constraint is increasingly the "Memory Wall."[44] Over the past two decades, processor speeds have grown roughly 90,000-fold, but memory (the system that feeds data to the processor) has only improved 30-fold.[45] Fast, expensive chips sit idle, simply waiting for data. The problem has grown so severe that in advanced AI chips, moving data to where it gets processed consumes more energy than processing it.[46]

On the supply side, the returns from further process scaling are rapidly diminishing, constrained by both physical limitations and economic realities. At atomic scales, quantum tunneling and leakage currents erode performance gains. Static random-access memory (SRAM) scaling has fallen far behind logic circuits, effectively cancelling the benefits of area reduction.[47] Development costs have exploded, as a single 5 nm design costs roughly $500 million, ten times the cost at 28 nm, and market projections for 2 nm exceed $700 million.[48] Worse, the unit cost curve has inverted. At 2 nm, 300 mm wafer costs rise approximately 50 percent over 3 nm, yet transistor density improves only 15–20%.[49] For mainstream applications not requiring peak computational performance, continued investment in the most advanced process nodes is no longer economically justified.

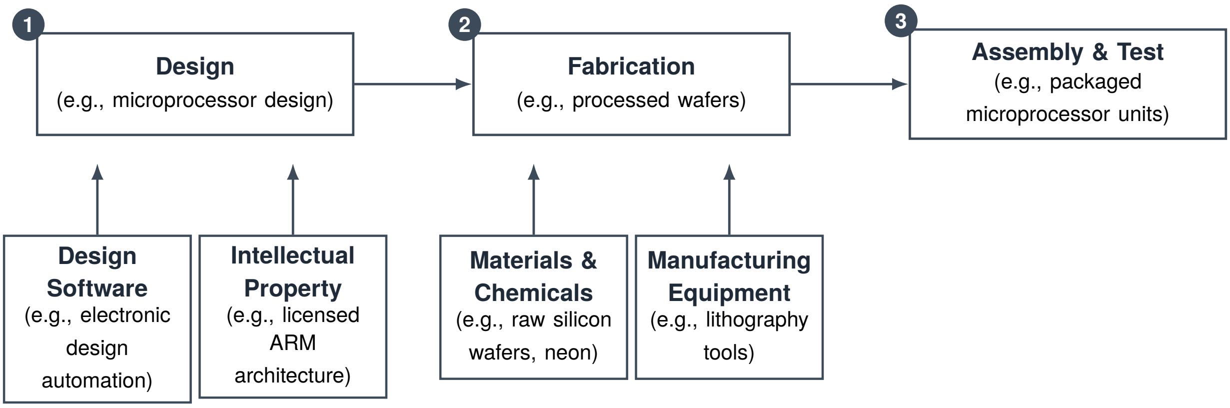
Firms along the semiconductor value chain are responding to this architectural shift. A critical objective for many is to shorten the physical distance between memory and compute cores and reduce the exorbitant energy costs of data transfers. At the same time, advanced packaging has upended the traditional structure of the value chain, blurring the lines between its upstream, mid-stream, and downstream segments.

This chapter develops an analytical framework for understanding advanced packaging as a strategic and regulatory object, not merely a technical one. Its central contribution is a three-pathway classification that differentiates advanced packaging approaches by technical capability, cost structure, division of labor, and regulatory exposure under the current U.S. export control regime. This framework demonstrates that the existing export control regime is node-centric, and the most cost-accessible pathway operates almost entirely outside its reach. The chapter then examines the engineering constraints that dictate the extent to which firms can travel along this pathway, and maps the supply chain chokepoints where regulatory leverage does and does not apply.

2.2 Restructuring the Semiconductor Value Chain

The traditional semiconductor value chain once followed a clear vertical division of labor. Upstream fabless firms designed the logic, and midstream foundries fabricated wafers. Downstream OSAT firms handled packaging and testing. Under this framework, back-end packaging was a supporting player for the upstream and midstream portions of the value chain. Because back-end processes were labor-intensive, technologically modest, and governed by relatively permissive environmental standards, Taiwan and later China were able to build large-scale packaging clusters. Figure 2.1 illustrates the traditional upstream-downstream relationship in the semiconductor value chain.

Figure 2.1. Simplified Semiconductor Value Chain



Source: Authors' adaptation based on a simplified semiconductor value-chain framework.[50]

Advanced packaging has disrupted this tidy division. As heterogeneous integration has matured, a distinct middle-end of line (MEOL) process has emerged between wafer fabrication and packaging. This middle ground is now the principal battleground for signal efficiency, interconnect density, and power management. The old labels of "wafer fabrication" and "packaging and testing" no longer capture the competitive landscape.

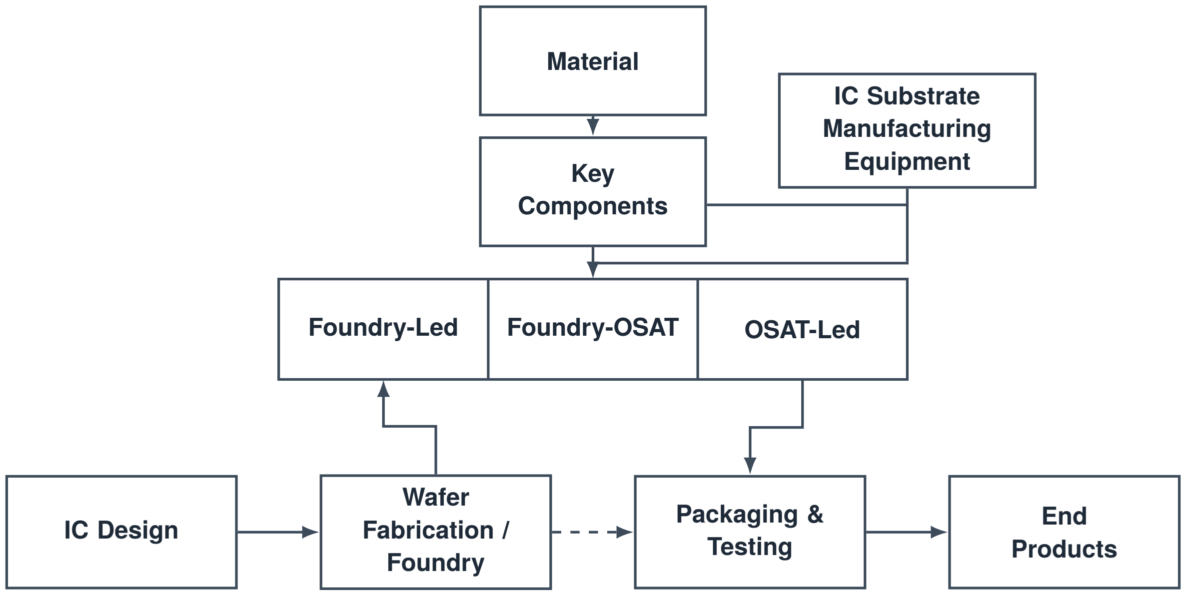
Foundries are pushing downstream. Foundries are extending their reach into what once was exclusively the packaging domain. For example, TSMC's CoWoS platform integrates logic chips and HBM on a silicon interposer. The reason is that a key technical divide lies in the interposer itself, which requires foundry-grade 65 nm processing—including Through-Silicon Via (TSV) and Redistribution Layer (RDL) steps. This is a capability that TSMC controls end-to-end. The subsequent bonding of the interposer to the organic substrate is partly subcontracted to OSATs such as ASE and Amkor.[51] NVIDIA, Broadcom, AMD, Google, Amazon, and MediaTek are all customers of TSMC's CoWoS platform.[52]

OSATs are moving upstream. Facing foundry encroachment, traditional OSATs are building proprietary capabilities to remain indispensable. ASE Group illustrates the dynamic by serving as a subcontractor for TSMC's CoWoS back-end work while concurrently developing its own fan-out panel-level packaging (FOPLP) and fan-out chip on substrate (FOCoS) technologies.[53] The result is a relationship of *co-opetition*—simultaneous collaboration and competition.[54] Representative cases include AMD partnering with ASE and Powertech to develop FOPLP. Both illustrate how OSATs are leveraging market trends to move into technical territory once reserved for foundries.

Accordingly, the critical nodes of advanced packaging are distributed, not concentrated. They span foundry-level core processes (silicon interposer fabrication), OSAT back-end capacity (die integration and fan-out packaging), and high-density substrate manufacturing. Each node depends on an interlocking web of materials, equipment, and chemicals. Thus, back-end packaging has evolved from a supporting role into a primary strategic chokepoint in the semiconductor ecosystem.

Advanced packaging's restructuring of the value chain requires a fundamentally different method of viewing supply chain relationships. This new perspective should capture the extent to which inter-node dependencies enable (or constrain) both the technological advancement and volume production of advanced packaging. Figure 2.2 maps the advanced packaging supply chain, showing the upstream-downstream relationships and the strategic positioning of each node. Historically, these nodes were long treated as secondary to front-end fabrication. However, as system-level performance increasingly depends on advanced packaging to overcome scaling limits, their strategic value has fundamentally shifted. The dependence of AI training and inference workloads on GPUs built with advanced packaging processes has made them inextricably linked to high-performance computing infrastructure. The regulatory frameworks built around the old division of labor have not kept pace with this restructuring—a gap that the three-pathway analysis in the following section illuminates.

Figure 2.2. Advanced Packaging Supply Chain



Source: Authors' compilation.

2.3 The Diverse Pathways of Advanced Packaging

The performance yielded by advanced packaging stems from a simple physical principle: shorter distances between chips mean lower signal latency, less resistive loss, and less heat buildup. The result is better overall system performance, without advancing the process node. Three distinct pathways have emerged in pursuit of these performance objectives, each with different cost structures, supply chain dependencies, and implications for regulatory leverage.

Pathway One is foundry-led, Pathway Two splits responsibility between foundries and OSATs, and Pathway Three is OSAT-led. The distinction matters because customers are attracted to a certain pathway due to their I/O density, line width precision, reliability, cost, and supply requirements (see Table 2.1). Moreover, from an export-control perspective, the three pathways differ in how readily they can be regulated: foundry-led processes offer the most obvious points of regulatory leverage; OSAT-led processes, the fewest.

Table 2.1. Technology Characteristics of the Three Advanced Packaging Pathways

Technology Pathway	Representative Firms / Platforms	Technology Characteristics
Pathway One: Foundry-Led	TSMC: CoWoS-S, SoIC; Intel: EMIB; Samsung: X-Cube	Wafer-level lithography; TSV ultra-fine pitch: $< 2\ \mu\text{m}$
Pathway Two: Foundry–OSAT	TSMC: CoWoS-R/L, InFO; ASE: FOCoS-Bridge; Amkor: SWIFT HD	Organic substrate + medium-precision RDL: 5–20 μm
Pathway Three: OSAT-Led	ASE: FOCoS, FOPLP, FC-BGA, SiP; Amkor: FC-BGA, SiP; JCET: FOPLP; Innolux: G3.5 FOPLP	PCB/substrate upgrade; large panel; wider RDL $>$ 20 μm

Table note:

a. The “Technology Pathway” classification in this table is based on the collaboration model among firms in the packaging process rather than on specific technical specifications, platform brands, or product names. Because the classification follows the division of labor rather than fixed technical parameters, the RDL precision, interconnect density, and material specifications associated with each pathway will continue to improve as process technology evolves. Accordingly, the specifications listed in the “Technology Characteristics” column reflect the state of the art as of 2025–2026 and should be updated periodically rather than treated as permanent threshold values.

b. Some firms operate across Pathway Two and Pathway Three depending on the product line. This is not an exception to the classification but a reflection of how firms flexibly switch collaboration roles in response to market demand. ASE is illustrative. Its standard FOCoS product line, in which ASE independently completes all packaging steps, falls under Pathway Three. However, FOCoS-Bridge with TSV (announced in 2025, supporting HBM3 × 4 with a package size of 85 mm × 85 mm) embeds an externally supplied silicon bridge die for critical die-to-die interconnection, with ASE handling assembly and substrate integration—a Pathway Two division of labor.[55] Amkor’s SWIFT HD platform similarly relies on foundry front-end RDL processing (Pathway Two), while its FC-BGA and SiP product lines represent Amkor’s core independent packaging capability (Pathway Three).[56]

c. Certain TSMC InFO deployments involve collaborative arrangements with ASE's back-end packaging operations: the foundry completes front-end InFO RDL processing, and the OSAT handles substrate bonding and system-level integration testing—a typical Pathway Two division of labor. However, both parties also compete directly in the high-end AI GPU packaging market. This co-opetition dynamic is accelerating each side’s push toward technological self-sufficiency and highlights the broader restructuring underway in the semiconductor supply chain.

d. Among the Pathway Three firms listed, Innolux is a display panel manufacturer that has crossed over into the packaging domain as a new entrant. Its G3.5 FOPLP production line (620 mm × 750 mm) offers roughly seven times the area of a standard 300 mm wafer, representing the leading edge of FOPLP's evolution toward large-area, low-cost manufacturing. Its process is entirely self-directed, consistent with the Pathway Three definition.

Source: Authors’ compilation.

Driven by the need for maximum density, Pathway One is dominated by foundries such as TSMC, Intel, and Samsung using wafer-level processes—silicon interposers, TSV, and 3D stacking—to deliver the tightest inter-die distances and highest I/O density on the market. With line widths reaching 1–2 μm or finer, these technologies are purpose-built for integrating high-power GPUs and AI accelerators with multiple HBM stacks. However, the trade-off is high cost. Because TSVs, wafer-level RDL, and precision die stacking are expensive processes with high yield risks, this pathway is strictly reserved for high-ASP (average selling price) products, including flagship AI GPUs and premium server processors.

Seeking balanced performance, Pathway Two pairs foundries and OSATs around 2.5D or fan-out packaging using organic substrates and medium-precision RDLs (5–20 μm). In this collaborative model, foundries handle the critical wafer-level steps, while OSATs manage back-end assembly and testing. The result is markedly better bandwidth and latency than traditional FC-BGA, achieving a sweet spot in pricing that works for mid-to-high-end networking, server, and AI ASIC applications where both performance and cost matter equally.

Finally, prioritizing cost optimization, Pathway Three is championed by OSATs such as ASE, Amkor, and JCET, by building upon existing PCB and substrate supply chains. Representative technologies—FOCoS, FOPLP, high-end FC-BGA, and organic-substrate SiP—utilize wider line widths of 8–25 μm. While interconnect performance is lower than the other two pathways, it offers unmatched cost efficiency and supply flexibility. Nonetheless, a primary engineering challenge persists in this approach: warpage. The coefficient of thermal expansion (CTE) mismatch between silicon dies and organic substrates causes warpage during thermal cycling, and this deformation worsens as package size increases, making it a significant barrier to scaling. These differences in technical capability and division of labor produce distinct cost profiles, as shown in Table 2.2.

Table 2.2. Advanced Packaging Cost Comparison

Technology	Pathway	Application Tier	Unit Cost (USD/package)	I/O Density / Pitch	Primary Source (anchor)
CoWoS-S (2.5D Si interposer)	One	AI GPU (H100-class, ~814 mm^2)	$650–950	Extreme / 1–2 μm	TechInsights H100 teardown (2023); Morgan Stanley (2024-01); Barclays (2024-12); JPMorgan (2024-12); Yole Intelligence (2024).
CoWoS-L (local Si bridge + RDL)	One	AI GPU (B200/GB200-class, ~1,000 mm^2)	$1,100–1,800	Extreme / 1–2 μm	Barclays (2024-12); JPMorgan (2024-12); Yole Intelligence (2024).
SoIC — process-only (3D stacking)	One	V-Cache, HBM stacking	$80–200/stack (excl. HBM die)	Extreme / $<$ 1 μm	AMD X3D retail premium; SemiAnalysis (2024-02).
SoIC — with HBM die (full module)	One	Complete HBM stack	$450–850/stack	—	SK hynix HBM3E pricing (2024); Yole Intelligence (2024).
InFO (Fan-out WLP)	Two	Apple A-series mobile SoC	$8–15	High / 5–10 μm	Yole InFO model (2023–24); Counterpoint A17 Pro analysis (2023-11).
CoWoS-R (networking ASIC)	Two	Mid-to-high-end networking / AI ASIC	$350–700	High / 2–5 μm	Barclays (2024-12); JPMorgan CoWoS-R analysis (2024-12).
Amkor SWIFT HD	Two	Mid-tier AI ASIC / server	$20–60	Med-high / 5–15 μm	Amkor SWIFT HD Technology Brief (2023).
CoPoS (panel-level, pre-HVM)	Two	Next-generation networking ASIC	$200–450 (volume data to be confirmed)	High / 5–10 μm	TSMC CoPoS technology briefing; Broadcom ASIC packaging estimates (Barclays 2024).
FC-BGA — consumer-grade	Three	Consumer electronics, mobile CPU	$5–15	Medium / 15–25 μm	Shinko pricing; Ibiden/Unimicron ASP (2022–24).
FC-BGA — server/HPC-grade	Three	AMD EPYC, Intel Xeon	$18–45	Medium / 15–25 μm	IC Insights Intel supply-chain analysis (2023); Barclays (2024-12).
FOCoS	Three	Mobile SoC, mid-to-high-end networking	$12–25	Med-high / 8–15 μm	ASE Investor Day (2023); IMAPS paper (2023).
FOPLP (pre-HVM)	Three	Mobile / networking (post-scale)	$12–25 current; $5–10 approaching post-wafer yield	Med-high / 8–20 μm	Innolux G3.5 roadmap (2024); SEMI FOPLP cost model.
mSAP HDI substrate	Two / Three	Networking / mid-tier server	$8–20; $20–50 for 800G / 112G high-density	Med-high / 10–15 μm	Ibiden/Unimicron ASP; TTM/Tripod pricing (2023–24).
China OSAT scenario (FC-BGA/FOCoS)	Three	Domestic substitution	$4–10	Same as FC-BGA/FOCoS	JCET 2023 annual report; TFME disclosed pricing; CSIS/SIA (2024).

Table note: All figures represent packaging-process costs, excluding silicon die, unless otherwise noted. CoWoS-S cost scales linearly with interposer area at approximately USD 0.7–1.2/mm^2. FOPLP cost reductions are realized only once panel yield matures above 90 percent; 2025–2026 has not yet reached HVM scale. CoPoS remains in early volume-production ramp and should be cited with caution.

Source: Authors' compilation based on company disclosures, teardown estimates, analyst reports, and open-source reporting.[60]

Three price bands in the cost gradient have distinct regulatory implications. The $650-1,800 band corresponds to AI/HPC flagship products covered by current ECCN 3A090 scope, and controls hold this segment effectively. The $200-700 band corresponds to Pathway Two hybrid applications, where coverage is partial under the "front-end gated, back-end open" division. The $4-45 band is Pathway Three's main battleground. Under Chinese OSAT and FOPLP configurations, it is further pressed down to $4-10, the thinnest segment of EAR coverage and the cost-feasibility basis of China's asymmetric breakout strategy. Unit cost shows what each pathway costs; cost-structure distribution shows where cost concentrates and that determines where regulatory leverage applies. The table below compares six cost components across the three pathways, with an "Aggregate Front-End Controlled Cost" row mapping directly to current EAR scope.

Table 2.3. Cost Structure Breakdown by Pathway

Cost Item	Pathway One: Foundry-Led (CoWoS-S)	Pathway Two: Foundry+OSAT (CoPoS)	Pathway Three: OSAT-Led (FO-CoS/ABF)
Si interposer / substrate	45–52% (controlled front-end)	20–30% (partially controlled)	15–28% (uncontrolled)
Wafer-level processing (TSV, RDL, CMP)	15–20% (controlled front-end)	8–14% (controlled front-end)	N/A (no wafer-level steps)
Assembly & bonding	22–28%	30–35% (mostly uncontrolled)	42–52% (largest single line item; uncontrolled)
Testing & verification	8–12%	10–14%	5–10%
Yield loss (effective cost share)	10–16% (CoWoS at 85–92% yield)	7–11% (InFO at >94% yield)	4–8% (FC-BGA at >96% yield)

Cost Item	Pathway One: Foundry-Led (CoWoS-S)	Pathway Two: Foundry+OSAT (CoPoS)	Pathway Three: OSAT-Led (FO-CoS/ABF)
CAPEX depreciation	High (single line $5–10B / 5–7 yr amortization)	Medium (foundry front-end + OSAT back-end split)	Low–Medium (incremental upgrade on existing PCB/substrate lines)
Indirect costs	Medium	Medium–Low	Low
Aggregate Front-End Controlled Cost[*]	60–72%	28–44%	0%
Corresponding EAR Control Scope	High coverage (Dec. 2024 IFR + ECCN 3A090)	Partial coverage (FDPR covers front-end RDL; OSAT assembly mostly uncontrolled)	Near-zero coverage (transactional DD only)

Table note:

a. Percentages indicate each cost item's share of total advanced packaging costs for the given pathway, not overall chip cost. Ranges reflect typical order-of-magnitude behavior; midpoints approximate 100 percent per pathway.

b. [*]The "Aggregate Front-End Controlled Cost" row sums midpoints of the Si interposer/substrate and wafer-level processing rows, mapping to the December 2024 IFR and ECCN 3A090 control scope.

c. All figures are calibrated against IMAPS 2.5D and 3D Packaging Cost Breakdown (Palesko & Lujan 2016); Fan-out Packaging Cost Analysis (Lujan 2023); TechInsights H100 BOM teardown (2023); Morgan Stanley CoWoS Economics (2024-01); Barclays Advanced Packaging Cost Structures (2024-12). Entries are literature-consistent approximations, not audited figures.

d. "CAPEX depreciation" and "Indirect costs" are expressed as qualitative levels, reflecting limited public visibility into firm-level accounting.

e. "Yield loss" reflects effective cost share attributed to non-perfect yield, inferred from published 2.5D/3D and fan-out yield sensitivities.

f. The table is intended to compare cost-structure profiles under current mainstream HVM assumptions and should be used for strategic and policy analysis only, not transactional pricing.

Source: Authors' compilation of several sources.[61]

2.4 China's Asymmetric Breakout Strategy: Pathway Three

China's concentration on Pathway Three is not a fallback imposed by resource constraints, rather it is a deliberate choice. Three conditions converge to make it so. First, cost feasibility. Chinese OSATs have driven unit packaging costs to $4-10 at volume scale, making Pathway Three commercially viable at the domestic market's required depth. Second, regulatory exposure. Pathway Three carries zero front-end controlled cost, placing it almost entirely outside EAR reach. Third, upward extensibility. Chinese firms can expand into Pathway Two's OSAT-handled assembly and integration steps without accessing the controlled front-end equipment that defines Pathway One. Together, these conditions make Pathway Three not merely accessible but strategically optimal. It is the right battlefield on which to concentrate effort.

Within this cost-stratified landscape, the relatively accessible technical thresholds of Pathway Three offer a viable entry point for China's semiconductor sector. Benefiting from a policy environment conducive to supply chain localization, Chinese OSATs are capitalizing on the cost-optimized nature of Pathway Three to secure high-volume commercial contracts. This base load capacity ensures their continued integration into the global packaging supply chain. Furthermore, as leading global facilities face capacity constraints driven by surging AI computing demands, Chinese manufacturers have emerged as a viable alternative to accommodate the resulting spillover demand. The revenues generated are being systematically reinvested into R&D and process upgrades, serving as a foundational step for accumulating critical technical expertise.

From a broader supply chain perspective, China is also executing a comprehensive domestic replacement strategy across the entire packaging ecosystem.[62] Catalyzed by export controls, Chinese firms are actively localizing key advanced packaging inputs across multiple tiers. This localization effort spans upstream materials—packaging chemicals such as EMC and DAF, and ongoing attempts to develop alternatives to critical ABF build-up films—as well as core manufacturing equipment, evidenced by emerging domestic prototypes in thermal compression bonders (TCB) and laser drilling systems.[63] Evaluating China's advanced packaging trajectory therefore requires moving beyond a narrow focus on single-point technological breakthroughs at the final integration layer. A comprehensive assessment must instead scrutinize the vulnerabilities and progress across every node of the supply chain—from foundational materials to core manufacturing equipment—determining how effectively China can mitigate foreign dependencies as it attempts to migrate from Pathway Three toward the more complex, high-density architectures of Pathway Two, and ultimately, Pathway One.

China's current strategy to surmount American restrictions on its AI ambitions echoes the parable 田忌賽馬 (*tianji saima*, or "Tian Ji's Horse Race") which dates back to the Warring States Period. During a series of horse races, General Tian Ji, advised by the strategist Sun Bin, raced his weakest horse against his opponent's strongest, his strongest against the opponent's middling, and his middle against the weakest. By conceding the first race, the general focused his victories on the other two races, resulting in a cumulative victory for him. The lesson is that applying asymmetry, rather than engaging in head-on confrontation, creates a path toward victory. Accordingly, China's strategy rests on two reinforcing pillars.

Pillar One: System Integration as a Substitute for Process Leadership. China cannot currently produce a single chip that competes with the United States at the most advanced nodes. Instead, it is leveraging its highest-attainable advanced dies—manufactured domestically despite equipment constraints—and using advanced packaging to interconnect multiple chips at high density. The goal is to close the performance gap at the system level rather than the wafer level. This direction happens to align with the global industry's post-Moore's Law trajectory. The difference is that for China, export controls have accelerated this approach from a natural industry evolution into an urgent strategic necessity.

Pillar Two: Leveraging Downstream Industrial Depth. China has spent decades building scale in the lower tiers of the semiconductor value chain, such as OSAT, substrate manufacturing, and PCB production. Rather than competing solely on cost, China is now actively repurposing this massive industrial foundation to support complex heterogeneous integration. This extensive baseline ecosystem provides the indispensable manufacturing infrastructure. When mobilized by aggressive state policy support, this foundation enables national champions to rapidly scale chiplet-based AI architectures.

The strategic objective is clear: even with advanced-process sources cut off, China aims to provide "good enough" computing infrastructure for domestic AI training and inference. Beijing has not abandoned the pursuit of leading-edge nodes. But with AI demand surging, advanced packaging acts as a vital compensatory mechanism, allowing the integration of available advanced chips to squeeze out maximum viable system performance faster. The resulting dual-track strategy—defined by a desire to achieve functional viability now and catch up on the process level over time—is designed to buy time and accumulate bargaining leverage. China's state-directed industrial policy apparatus and national champion selection that enables this strategy is examined in Chapter 3.

In this regard, advanced packaging is no longer a technical niche. It is the vehicle in China's campaign to break out of what Beijing's leaders see as *technological containment* and sustain its position in the global AI race.

2.5 From Lab to Fab: Physical and Engineering Challenges

The two pillars of China's asymmetric strategy each carry a structural ceiling. That ceiling is defined not by policy but by physics. Three tightly coupled engineering challenges govern how far Pathway Three can be scaled and under what conditions migration toward Pathway Two becomes feasible: interconnect precision at the chip level, warpage control at the interposer and substrate level, and thermal management at the system level. These are not isolated bottlenecks, and a design choice at one level can trigger cascading effects at others. Together, they form the gate between laboratory demonstration and high-volume production, and the basis on which leading firms build their moats. For policymakers, these challenges provide a concrete framework for assessing the limits of China's packaging-based strategy. Table 2.4 summarizes and assesses the challenges of each pathway.

Table 2.4. Physical Challenges and Policy Assessment by Pathway

Challenge	Pathway One: Foundry-Led	Pathway Two: Foundry+OSAT	Pathway Three: OSAT-Led
Precision	Highest (hybrid bonding, sub-nm control); deepest moat	Medium (micro-bumps + mid-precision RDL); foundry-dependent	Manageable (wider pitch); I/O density ceiling
Warpage	Si interposer buffers chips; large-area interposer–substrate mismatch persists	Molding compound buffers partially; fine-tuning required	Most severe: silicon on organic, multi-fold CTE gap; size-constrained
Thermal	Highest heat flux; liquid cooling or microfluidics mandatory	Better distribution; liquid cooling for high-end	Lowest density; air cooling viable; EMC bottleneck in large packages
Applications	AI GPUs, HBM, HPC servers	Mid–high AI ASICs, networking, CPUs	Mobile, networking, consumer
China Catch-Up	Extremely hard: front-end environment needed; export-controlled	Hard: deep front-end partnership needed	Moderate: current equipment supports it; ceiling limited

Source: Authors' compilation.

2.5.1 Chip Level: Interconnect Precision

The core challenge is the continued miniaturization of bump pitch, the spacing between chip-to-chip or chip-to-interposer connections. Early flip-chip packages used pitches of roughly 100 μm. Today's micro-bumps operate at tens of microns. Next-generation targets are in the single digits, and each step drives an exponential increase in process difficulty.

Below ten microns, conventional solder ball processes hit their physical limits. Hybrid bonding is the successor technology because it eliminates micro-bumps entirely by bonding copper pads directly to one another while simultaneously fusing the dielectric and metal layers. The result is higher interconnect density and lower resistance at finer pitches.[64]

However, the process demands are severe. Dielectric surface roughness must be controlled to sub-nanometer levels. Copper pad dish depth must stay within single-digit nanometer tolerances. Even micron-scale particle contamination at the bonding interface can create voids many times larger than the contaminant itself, causing electrical failure.[65] Cleanroom standards must mirror those of front-end wafer fabs, and alignment accuracy must reach the hundred-nanometer range.[66]

These requirements define the clearest division of labor across the three pathways. Pathway One (foundry-led) uses complete hybrid bonding flows in front-end fab environments—the deepest technical moat. No OSAT can currently replicate this. Pathway Two (collaborative) relies on micro-bumps with medium-precision RDLs, requiring foundries to complete the critical front-end steps before handing off to OSATs. Pathway Three (OSAT-led) uses larger-pitch flip-chip or modified semi-additive process (mSAP) traces, manageable with existing equipment but capping I/O density gains.

2.5.2 Interposer and Substrate Level: Warpage Control

When layers of different materials are stacked, differences in their CTE become a critical problem.[67] Silicon has a very low CTE, and organic substrates can expand more than ten times as much. Copper traces and dielectric materials expand at different rates, adding further thermal mismatch and accumulating stress through high-temperature steps like annealing and reflow soldering.[68]

During repeated heating and cooling cycles, these mismatched layers act like opposing springs, generating warpage.[69] When warpage exceeds tolerances, fine-pitch solder joints crack or deform, degrading yield and causing early reliability failures.[70]

The three pathways face distinct warpage profiles. In Pathway One, a silicon interposer sits between the chips and the organic substrate, closely matching the CTE of the chips above. But the interposer still mismatches the substrate below—and the larger the interposer (as in multi-die GPU packages), the harder the warpage becomes to manage.[71] Pathway Two uses high-fill-rate molding compounds that provide intermediate CTE buffering, but careful tuning of layer thicknesses and material ratios remains essential.[72] Pathway Three faces the starkest challenge because silicon dies sit directly on organic substrates with CTE gaps of several-fold. This is the core physical constraint limiting OSAT-led approaches from scaling to larger packages.[73] These problems will become increasingly pronounced as AI chip systems scale up in size.

Warpage control imposes a technical ceiling on Chinese OSATs. Any pursuit of higher interconnect density requires advancing both substrate material formulations and process control in parallel. This is a necessary condition for upgrading from Pathway Three to Pathway Two, and one of the principal engineering bottlenecks at present.

2.5.3 System Level: Thermal Management

As advanced packaging compresses chip distances and increases functional density, power density per unit area has become the binding constraint, rather than total power alone. In CoWoS packages, heat flux density can approach or exceed 1 kW/cm², concentrated in a small fraction of the total package area. The result is extreme thermal hotspots[74] that raise junction temperatures and thermal gradients, accelerating electromigration and material fatigue. Traditional air cooling cannot keep pace.

Three thermal management approaches have emerged in response. Direct liquid cooling places cold plates or channels in direct contact with the package and is the current standard for high-power AI servers. Embedded microfluidic cooling uses phase-change boiling to push dissipation limits by routing channels into the chip or substrate itself.[75] Phase-change materials act as thermal buffers by absorbing transient power spikes.[76]

Thermal pressure varies by pathway. Pathway One faces the most extreme density and almost certainly requires direct liquid cooling or embedded microfluidics, with thermal-electrical co-optimization beginning at the chip design stage. Pathway Two spreads dies horizontally, improving heat distribution and offering more design flexibility. Pathway Three has the lowest power density since air cooling works for most applications, although the poor thermal conductivity of epoxy molding compounds (~0.8–1.0 W/m·K vs. silicon's ~150 W/m·K) can create localized bottlenecks in large-area packages.[77]

Thermal management challenges are relatively tractable at Pathway Three, where air cooling is widely available among Chinese firms. However, once a firm moves up to Pathway Two, the jump in power density requires a corresponding leap in thermal-electrical co-design capability. This is therefore no longer a packaging-assembly question alone, but one that requires integrated optimization of material selection, package architecture, and cooling system. Given China's current technology base, where single-die or chiplet performance is constrained by front-end process limits, the heat and power problems at the chip level become amplified at the system level—an unavoidable system-engineering challenge in any pathway upgrade.

2.6 Supply Chain Chokepoints and Regulatory Gaps

The three-pathway framework, the engineering constraints it generates, and the logic of China's asymmetric strategy all point toward the same policy question: where does regulatory leverage actually apply? Answering that question requires deconstructing the advanced packaging ecosystem tier by tier and identifying the points at which U.S. export controls hold, where they are partial, and where they are absent entirely. U.S. export controls successfully choke off advanced front-end equipment and final systems (such as AI GPUs and HBMs). However, Washington has overlooked the OSAT-led packaging approach (Pathway Three)—the very foundation from which Chinese firms are launching their catch-up efforts.

To operationalize this OSAT-led pathway, China relies heavily on a specific set of unmonitored supply chain tiers. The U.S. regulatory regime remains highly porous to Tier 1 upstream materials (ABF and BT resins), Tier 2 key components (ABF substrates), and Tier 3 back-end tools (laser drills). By funneling these unrestricted lower-tier inputs into domestic architectures, China can successfully integrate its highest-attainable advanced dies. While this packaging-driven approach cannot achieve true process leadership or perfect performance parity, it functions as a vital compensatory mechanism.

Crucially, because the foundational materials and equipment across Pathways One, Two, and

Three significantly overlap, these uncontrolled inputs serve a dual strategic purpose. They not only sustain current production but also allow China to accumulate critical engineering expertise in unrestricted areas, providing the essential technical stepping stones to upgrade toward the higher-density interconnects of Pathway Two and beyond. This dynamic highlights why addressing supply chain gaps is essential for American policymakers.

Table 2.5 provides a holistic map of the advanced packaging supply chain, identifying China's chokepoints and the extent of export control coverage. As the table demonstrates, the areas where China remains most vulnerable are precisely where BIS export controls are currently lacking. A comprehensive breakdown of these specific tier-by-tier dependencies can be found in the Appendix.

Table 2.5. Five-Tier Supply Chain Control Gap Overview

Tier	Key Firms	China Status	EAR Coverage	Policy Implication
1: Upstream Materials (ABF, BT resin, chemicals)	Ajinomoto (Japan) >95% ABF; MGC (Japan) BT; Henkel (Germany)	Cannot self-supply; pilot stage only	Not controlled	Tech gap × regulatory gap = top-priority new control node
2: Key Components (ABF substrates, Si interposers, HDI PCB)	Unimicron, Ibiden, AT&S, Nan Ya PCB, Shinko Electric. Top 5 firms hold 60% market share ABF substrates; TSMC/Intel interposers	Emerging production, but yield and capacity gaps remain in AI/HPC ABF substrates; HDI PCB self-sufficient; SMIC mid-tier interposers	ABF substrates not directly controlled	"Lock equipment = lock product" fails when materials are uncontrolled
3: Mfg. Equipment (deposition/etch, laser drill, bonders)	AMAT/Lam/KLA (U.S.); TEL (Japan); Besi (NL); ASMPT; Via Mechanics	NAURA leading domestic growth; PrecisioNext first CoWoS-grade TCB test	Dec. 2024 expansion; laser drill hardware still open	Control window narrowing as China substitutes domestically
4: Adv. Packaging (Foundry vs. OSAT)	TSMC/Intel/Samsung; ASE/Amkor/JCET/TFME	JCET XDFOI 2.5D in production for 4 nm chiplets; SJ Semi TSV; Wuyuan hybrid bonding	Foundry controlled; Jan. 2025 rules impose OSAT due diligence but leave physical equipment/materials outside EAR	Symptomatic vs. structural controls: DD rules target transactions rather than capabilities, leaving bypass capacity intact
5: Final Systems (AI GPU, HBM)	NVIDIA/AMD; SK hynix/Samsung/Micron	Ascend 910C ~60% of H100 via chiplet packaging; CXMT targets HBM3 by 2026	BIS controls AI GPUs and HBM	Compute thresholds miss chiplet-based circumvention

Table note: This is a summary table; see Appendix A for further details.

Source: Authors' compilation of several sources.

The five-tier classification reveals several important conditions in China's current advanced packaging supply chain. Each segment continues to exhibit a range of bottlenecks and gaps, and full domestic substitution is unattainable in the short term. At the same time, the framework exposes the gaps in current EAR coverage. While existing controls reach front-end processing, China's intent to use advanced packaging as a circumvention path is now clear. Based on this chapter's chokepoint analysis, China's breakout effort in advanced packaging will face significant obstacles. These critical nodes pose substantial engineering challenges that differ materially from those associated with front-end process scaling.

Chapter 3 | Institutional Acceleration: How China Converts Advanced Packaging into a National Compute Capability

Increasingly restricted by front-end constraints attributable to export controls and the laws of physics, China has utilized advanced packaging to sustain and scale AI compute. Since advanced packaging spans a multi-partite ecosystem—which includes equipment, materials, substrates, PCBs, and assembly and test—a single firm cannot construct it. Instead, the advanced packaging ecosystem requires a concerted top-down effort, guided by policy direction instead of being driven by markets alone. This is because such investments face high yield uncertainty, long payback periods, and require tightly coordinated progress across multiple segments of the supply chain, making them structurally unattractive under conditions of uncertainty. China's state-led advanced packaging strategy expedites project timelines, absorbs risk, and realizes engineering potential.

Accordingly, China's acceleration in advanced packaging is driven by a layered institutional structure between the central and local governments. Over the past few years, Beijing has shifted advanced packaging to the center of its semiconductor and AI development agenda. On the state level, capital and policy-based finance absorb yield, technical, and market uncertainties that private actors cannot shoulder. Local governments then translate state direction into production lines, execute project milestones, and deploy compute infrastructure. This layered structure has allowed advanced packaging to rapidly move from the policy margins to the core of China's broader AI buildout.

In effect, China is undertaking an accelerated form of industrial catch-up, driven by the country's whole-of-nation mobilization system (举国体制). China's concerted effort not only allows further innovations in AI compute, but it also exploits loopholes in the United States' export control framework which is primarily built around node-based restrictions. The following chapter traces how China's institutional architecture operates through policy realignment, capital deployment, demand-side coordination, and local implementation. Together, these mechanisms have converted advanced packaging from a technical possibility into an operational pillar of China's compute system.

3.1 Policy Redefinition: From Node Catch-Up to System-Level Breakout

China's advanced packaging policy gradually evolved within the broader governance framework guiding semiconductor development. Since the 2014 *National Integrated Circuit Industry Development Outline* (国家集成电路产业发展推进纲要), packaging and testing have appeared among China's designated development priorities.[78] However, in practice packaging and testing played a supporting role; they merely filled gaps in the industrial chain and facilitated progress in IC design and manufacturing.

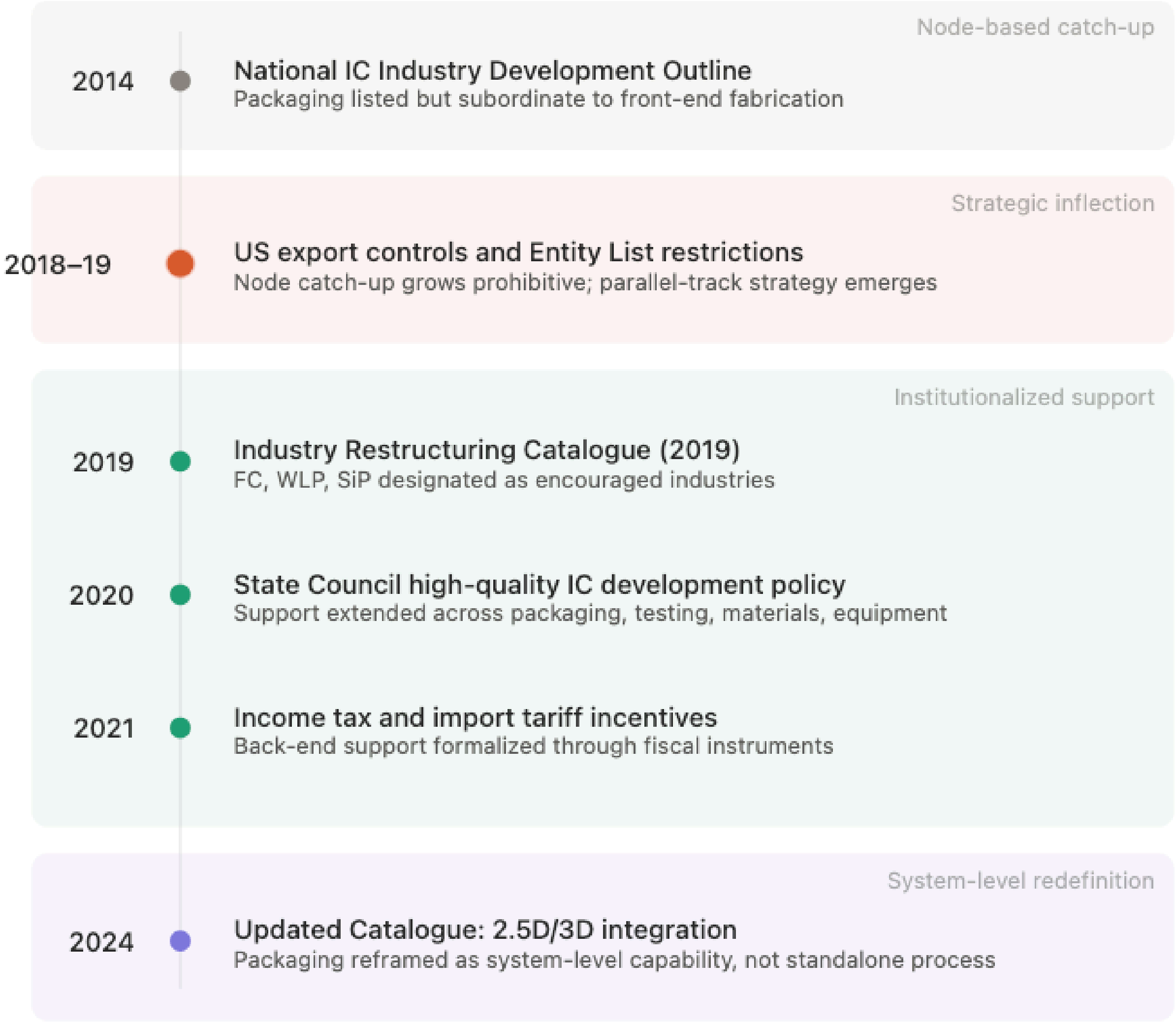
China's semiconductor policy hit an inflection point around 2018 and 2019, when the United States began imposing export controls on cutting-edge fabrication processes and designating Chinese firms and individuals on the Entity List. These actions cut off China's access to advanced semiconductors. Recognizing the increasing difficulties with catching up to the United States vis-a-vis chip nodes, China widened its semiconductor strategy. The hitherto single-track pursuit of node parity with the United States bifurcated. On a parallel track, China began maximizing system-level performance with their current hardware through innovations in architectural design and packaging interconnects.

State policy documents began to reflect this reorientation. The *2019 Catalogue for Guiding Industry Restructuring* (产业结构调整指导目录（*2019*年本）) designated specific advanced packaging processes as “encouraged industries,” includingflip-chip (FC), wafer-level packaging (WLP), and system-in-package (SiP).[79] In 2020, the State Council issued *Several Policies on Promoting High-Quality Development of the Integrated Circuit Industry and Software Industry in the New Era* (新时期促进集成电路产业和软件产业高质量发展的若干政策).[80] That document, in addition to a series of 2021 supporting measures on income tax and import tariff incentives, extended institutionalized support to packaging, testing, materials, and equipment.[81] These documents propelled the policy center of gravity toward establishing and sustaining an operational semiconductor supply chain.

Most recently, the *2024 edition of the Catalogue* (产业结构调整指导目录（*2024*年本）) explicitly redefined advanced packaging within China’s industrial strategy. The document includes “advanced packaging and testing integrating one or more technologies such as 2.5D and 3D” as an “encouraged” category.[82] The language no longer simply lists individual packaging formats. It instead emphasizes integration across multiple technologies, framing packaging as a component of system-level capability—the joint configuration of compute density, bandwidth, and energy efficiency—rather than a standalone process choice.

Across this trajectory, China’s evolution in advanced packaging policy exhibits a palpable institutional logic. Before, policy focused on compensating for weaknesses in front-end node development. Now, policy gravitates toward fortifying system integration. As export controls tightened, China reoriented its semiconductor strategy (see Figure 3.1). This pivot offers China more diverse policy options and faster cumulative returns than a sustained pursuit of front-end nodes would have. In other words, advanced packaging has moved from a low-margin, subordinate segment of China’s semiconductor industry toward a strategic node in China’s AI and compute development agenda.

Figure 3.1. Evolution of China’s Advanced Packaging Policy Framework



Source: Authors' compilation and analysis based on official Chinese government policy documents and open-source reporting.

3.2 State Capital: Risk Absorption as an Enabling Mechanism

Policy direction alone cannot sustain an industrial push of this scale. Industrial transition must be stimulated by the introduction of state capital into industries where private investment currently lacks the scale and time horizon to incubate. Constraints attributable to prolonged yield ramp-up cycles, immature domestic equipment and materials, high upfront costs, and uncertain payback timelines position advanced packaging as unattractive to private investors. To encourage development, state capital intervenes, underwriting the losses and delays that market-driven financing would not assume.

The National Integrated Circuit Industry Investment Fund (国家集成电路产业投资基金), more commonly known as the "Big Fund" (大基金), fills this role by converting capital into a policy instrument. Through equity stakes and long-term holdings, the fund lowers the threshold for continued investment in nascent technologies and unreliable production processes. Firms receiving Big Fund financing can continue progressing along learning curves toward production readiness. This enables firms to accumulate engineering experience under conditions of managed exposure rather than market exit.

The Big Fund's evolving investment structure tracks the policy trajectory described in Section 3.1. Phase I, established in 2014, focused on closing manufacturing capacity gaps. Roughly two-thirds of its capital went to IC fabrication, and packaging and testing received approximately 10 percent of the fund.[83] OSAT leaders JCET (长电科技) and TFME (通富微电) received investment at this stage, but primarily as strategic complements to front-end priorities.

Phase II of the Big Fund, launched in 2019, signaled an explicit reorientation as export control pressure mounted. The fund expanded in scale and began redirecting capital toward equipment, materials, and packaging as critical nodes within the supply chain. The fund's stated objective shifted from gap-filling toward building a more complete and resilient supply chain. While packaging and testing did not become the largest category for financial allocation, they became an explicit part of the supply-chain reinforcement agenda, reducing dependence on front-end processes.[84]

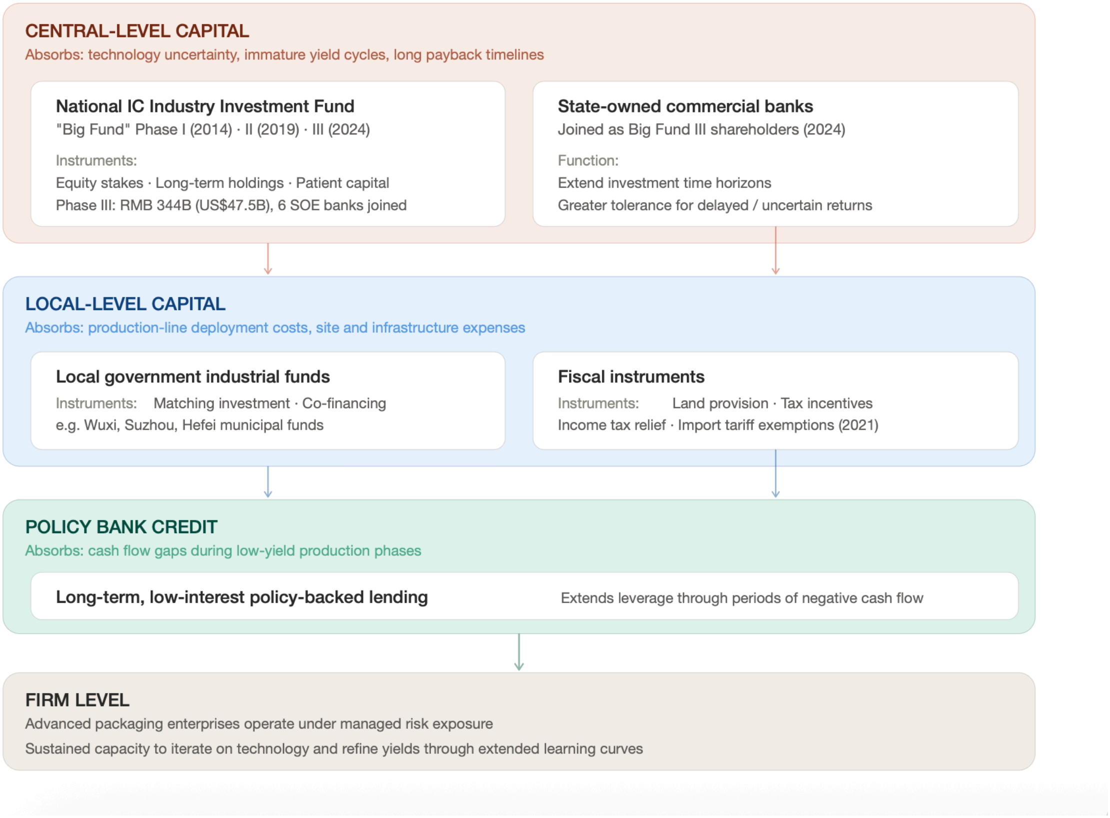
Phase III, established in 2024, represents an acceleration. This phase's registered capital of RMB 344 billion (US$47.5 billion) exceeds the first two phases combined.[85] For the first time, six major state-owned commercial banks joined as shareholders, giving the fund longer investment horizons and greater tolerance for delayed or uncertain returns.[86]

Early investment activity underscores these priorities in practice. Funds under Phase III participated in a financing round for Piotech Jianke (拓荆键科), an equipment supplier focused on 3DIC advanced packaging.[87] The company's product portfolio spans wafer-to-wafer and chip-to-wafer hybrid bonding, fusion bonding, and associated metrology equipment, addressing core bottlenecks in 2.5D and 3D integration.

The Big Fund's impact compounds through coordination with local government industrial funds and policy-backed lending. Central capital shoulders the most uncertain technology wagers. Local governments absorb production-line deployment costs through land provision, tax incentives, and matching investment. Policy banks extend leverage through long-term, low-interest loans. This layered equity-and-credit structure, as shown in Figure 3.2, allows advanced packaging projects to remain operational even during phases of low yields and negative cash flow—conditions under which private financing would withdraw.

From an institutional design standpoint, the role of state capital extends beyond funding provision. By redistributing risk across public balance sheets and extending investment time horizons, it converts investments that markets cannot fund into investments that firms can bear. By holding equity, state capital removes the repayment clock that would otherwise force firms toward near-term returns. This sustains the capacity for firms to continually iterate on technology and refine yields, even where the process frontier remains out of reach.

Figure 3.2. Layered Risk-Absorption Architecture in China's Advanced Packaging Capital Structure



Source: Authors' analytical framework based on policy documents, industry analysis, and open-source information.

3.3 Demand-Side Institutionalization: Locking in Compute Deployment

China's advanced packaging trajectory is distinguished by the deliberate construction of "demand-side lock-in." Through a series of national compute infrastructure programs, China has embedded advanced packaging as a critical component of AI and digital infrastructure. In doing so, the Chinese government has generated a consistent demand for the upscaling of advanced packaging technologies.

From the designation of "New Infrastructure Construction" (新型基础设施建设) as a strategic priority in 2020, China has progressively built out a national-scale compute architecture.[88] Successive initiatives include the National Integrated Big Data Center System (全国一体化大数据中心体系), the East-to-West Computing Resource Transfer project (东数西算), and the ongoing construction of a National Integrated Computing Network (全国一体化算力网).[89] Together, these programs elevate computing power to the status of critical national infrastructure, comparable to energy and transportation. At the policy level, they bind compute development directly to AI, cloud computing, and the digital economy.

Designing compute nodes at this scale requires simultaneously optimizing for high-speed interconnects, modular scalability, and sustained power and thermal management. These engineering challenges are situated at the packaging and system-integration level, not at the level of individual chip fabrication. Because these challenges determine whether compute infrastructure can operate reliably at scale, deployment criteria have shifted toward system-level deployability, operational stability, and supply-chain controllability. Under these evaluation parameters, chips domestically available to Chinese firms, combined with advanced packaging, offer a viable performance pathway.

National and provincial AI data centers (智算中心) are among the primary channels through which this demand is constructed and scaled.[90] Typically led by local governments and state-owned investment platforms (or state owned enterprises, SOEs), these data centers carry public mandates for regional AI training, inference, and industrial enablement. Dedicated budgets and long-term operational priorities support their construction and expansion.[91]

Beyond AI data centers, SOEs and major state-owned firms constitute another significant channel through which compute demand is institutionally anchored across strategic sectors such as energy, transportation, finance, and telecommunications.[92] Policy directives that encourage, and in some cases require, these entities to prioritize evaluation and adoption of domestic compute solutions aim to progressively increase the share of domestically produced hardware and software in their operations.[93]

For instance, energy-rich provinces where data centers are concentrated, such as Gansu, Guizhou, and Inner Mongolia, have begun using electricity subsidies to lower operating costs for domestic compute solutions. These incentives can be substantial: electricity price subsidies for large data centers can reach nearly half of standard rates. Moreover, data centers using domestic AI chips are reportedly more likely to qualify for such incentives.[94]

Demand-side lock-in advances through project-based mechanisms. Centralized procurement, unified validation programs, and pilot deployments distribute the early-adoption risks of emerging technologies across public institutions. Among domestic compute solution providers with the scale and system-integration capacity to serve these projects, Huawei's ecosystem is the most prominent. Public compute infrastructure deployment therefore provides a real-world operating environment for Huawei's products and the packaging and system-integration architectures they depend on.

Once operating at scale within public compute infrastructure, these systems become subject to sustained real-world validation. The result is a self-reinforcing cycle. Demand-side lock-in creates a learning loop in which packaging and integration capabilities are tested, corrected, and iteratively improved through actual deployment. Advanced packaging production lines can sustain continuous output and engineering feedback even when yields remain low and costs high because public compute projects shoulder the financial and technological risks and generate real-world experience needed to improve faster.

Predictable deployment demand lowers the decision threshold for firms weighing whether to continue investing. Across the broader industrial system, this process ensures that packaging capabilities evolve in step with AI application demand—setting the institutional conditions under which firms with system-integration capabilities can transition from technical experimentation to scaled deployment.

3.4 Local Implementation: Strategic Selection and the Emergence of National Champions

Local governments ultimately determine which firms achieve scale. Local governments at the provincial, municipal, and sub-municipal levels possess significant latitude and resources to support firms. By selecting projects, allocating production lines, and encouraging competition for resources, local governments facilitate the rise of industry "National Champions." Just as the "hundred flowers" pattern of decentralized local competition drove China's semiconductor development, the advanced packaging ecosystem is predicated on fierce competition between firms.[95]

The initial stage is always exploratory. Multiple localities invest in R&D, test competing technology combinations, and race to build production lines. Although this stage involves redundancies, including misallocated investments, it advances technical experience that positions firms supported by local governments to capitalize on emerging points of technological convergence.

Compared with earlier phases of China's semiconductor development, local competition has begun to shift toward what might be described as "simultaneous concentration and differentiation."[96] That competition is now consolidating around a smaller number of key clusters. For example, the Yangtze River Delta (Shanghai, Wuxi, Shaoxing), the Pearl River Delta and Greater Bay Area (Shenzhen), and central hubs such as Wuhan have continued to launch IC industry funds and projects.[97] Yet the logic governing capital allocation has shifted. The pace at which provinces establish new large-scale IC parent funds has slowed, and remaining funds are moving away from scale-driven investment toward allocation organized around specific project pipelines. Established local supply-chain ecosystems and the presence of anchor firms increasingly determine where capital flows.[98]

China's advanced packaging industry has thus moved from the exploratory stage toward a more structured division of capabilities across regions. The investment priorities of Big Fund Phase III, the buildout of national computing hubs, and the practical demands of the East-to-West Computing Transfer project have collectively formed a set of de-facto screening criteria.[99] Local projects that possess the potential to connect their technology to system-integration requirements and serve sovereign compute initiatives attract growing concentrations of capital and policy support. Conversely, projects that cannot deliver on these demands are ostracized from the national compute architecture.

The Pearl River Delta and Greater Bay Area exemplify this phenomenon. The region's mature PCB ecosystem, systems integration capabilities, and server and networking manufacturing base have positioned it as a hub for AI server and system-level packaging projects.[100] Local governments are no longer simply promoting capacity expansion. They now identify which technology pathways and firm clusters can serve the national compute agenda, and channel resources accordingly. Recent developments in Shenzhen further underscore this shift. The activation of a large-scale AI cluster built on domestic chips demonstrates how local governments are coordinating compute infrastructure deployment in alignment with national priorities.[101]

The layered process of central government direction, local government experimentation, and demand-driven convergence has produced China's advanced packaging national champions. Figure 3.3 and Table 3.1 map the geographic distribution and state capital linkages of firms across the advanced packaging value chain, from system anchors and OSAT providers to equipment, substrate, and memory nodes. Their emergence marks where China's advanced packaging ecosystem has moved from a collection of individual capabilities toward a system increasingly integrated into the country’s broader AI and compute deployment architecture.

Figure 3.3. Geographic Distribution of Key Firms in China’s Advanced Packaging Landscape

YANGTZE RIVER DELTA	
● JCET	Jiangyin, Jiangsu
● Tongfu Microelectronics	Nantong, Jiangsu
● SJ Semiconductor	Jiangyin, Jiangsu
● ACM Research	Shanghai
● AMEC	Shanghai
● Piotech Jianke	Jiaxing, Zhejiang
● WUS Printed Circuit	Kunshan, Jiangsu

PEARL RIVER DELTA	
● Huawei	Shenzhen, Guangdong
● Shennan Circuits	Shenzhen, Guangdong
● Victory Giant Technology	Huizhou, Guangdong
● Shengyi Electronics	Dongguan, Guangdong
● Kingboard Holdings	Hong Kong

Source: Authors’ compilation based on corporate filings and company disclosures.

Table 3.1. Key Firms in China’s Advanced Packaging Landscape: Technical Roles and State Capital Linkages

COMPANY	HEADQUARTERS	TECHNICAL ROLE	STATE CAPITAL
● System anchors — compute system integrators			
Huawei 華為	Shenzhen, Guangdong	Ascend AI chip + system integration	—
● Advanced packaging core — 2.5D / 3D / chiplet OSAT			
JCET 长电科技	Jiangyin, Jiangsu	Full-spectrum adv. packaging	Big Fund Central SOE
Tongfu Microelectronics 通富微电	Nantong, Jiangsu	FC-BGA, bumping, AMD partnership	Big Fund Local fund
Huatian Technology 华天科技	Tianshui, Gansu	SiP, TSV, bumping	Big Fund
SJ Semiconductor 盛合晶微	Jiangyin, Jiangsu	Wafer-level packaging, fan-out	Big Fund Local fund
● Bottleneck mitigation — equipment, process & substrate enablers			
Piotech Jianke 拓荆键科	Jiaxing, Zhejiang	Hybrid bonding, 3DIC process equip.	Big Fund
ACM Research 盛美半导体	Shanghai	Wet clean / electroplating equip.	Local SOE
Hwatsing 华海清科	Tianjin	CMP equipment	Central SOE
AMEC 中微公司	Shanghai	Etch / MOCVD (front-end enabler)	Local SOE
Shennan Circuits 深南电路	Shenzhen, Guangdong	IC substrate, high-speed PCB	Central SOE
WUS Printed Circuit 沪电股份	Kunshan, Jiangsu	High-freq. PCB / IC substrate	—
Kingboard Holdings 建滔集团	Hong Kong	Laminate / CCL material	—
● Server-level high-speed PCB & AI board layer			
Victory Giant Technology 胜宏科技	Huizhou, Guangdong	Server / AI accelerator PCB	—
Shengyi Electronics 生益电子	Dongguan, Guangdong	High-speed PCB for servers	Local SOE
● Memory integration node — bandwidth amplifier			
CXMT 长鑫存储	Hefei, Anhui	DRAM (HBM pathway)	Big Fund

Big Fund National IC Industry Investment Fund Central SOE Central state-affiliated capital

Local fund / SOE Provincial or municipal state capital — No identified state capital among top shareholders

Table note: Capital markers reflect top-10 shareholders as of latest available disclosure.

Source: Authors' compilation and analysis based on corporate filings and company disclosures.[102][103][104][105][106][107][108][109][110][111][112][113][114]

Chapter 4 | Capability Validation: How Advanced Packaging Translates into Deployable AI Compute

Policy mobilization and capital deployment do not solely constitute compute capability. Under conditions of constrained access to leading-edge nodes, advanced packaging has emerged as a primary pathway for sustaining AI compute growth in China. The viability of this pathway must be evaluated at the product level, through AI chip architecture, compute density, and the ability to support scalable deployment. This chapter concerns the application end, examining whether AI accelerators and the deployment architectures built around them entail advanced packaging's translation from an engineering possibility into operational compute capability.

Within China's compute ecosystem, Huawei is the central case through which this question is tested. It is one of very few Chinese companies that span chip design, system integration, and data center deployment within a single stack.[115] These capabilities extend across AI accelerator design (Ascend), software frameworks (MindSpore), server systems (Atlas), and model development (Pangu). Since its placement on the Entity List, Huawei has operated under sustained constraints on access to advanced process nodes and key equipment, making conventional node-based scaling largely unavailable as a performance strategy.

> *"For reasons we all know, we don't have access to advanced process nodes, so we've decided to focus our efforts on making breakthroughs by combining chips—essentially connecting more computing resources."*
> *— Eric Xu, Rotating Chairman, Huawei (Huawei Connect 2025)*[116]

Huawei's strategy in response to restrictions makes studying the firm analytically valuable. Its product evolution illuminates how engineering choices are made under conditions of restricted process access, institutional acceleration, and sustained state-driven compute demand.[117]

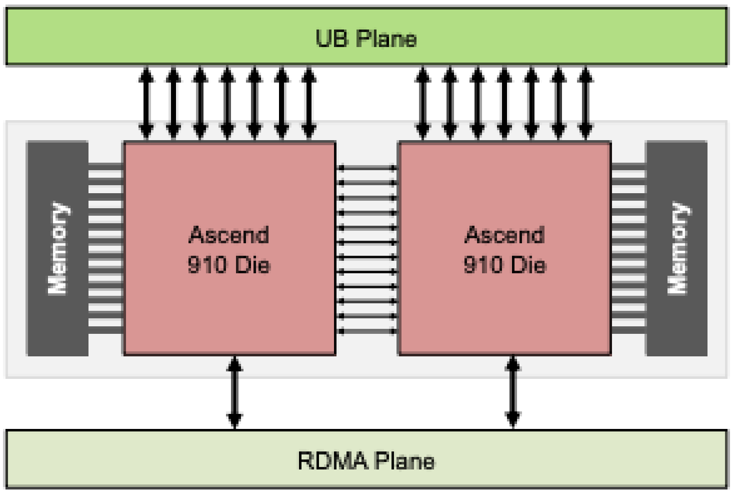
Analyzing Huawei's advanced packaging trajectory therefore doubles as a test of whether China's advanced packaging pathway has begun to produce deployable compute capability. The chapter examines this trajectory across Huawei's AI accelerator line, from deployed systems to emerging architectural directions and the ecosystem that supports them. It raises a policy question about whether export control frameworks designed around process-node restrictions adequately address this alternative pathway.

4.1 Deployed Systems: Advanced Packaging in the Ascend 910C

The Ascend 910C is Huawei's most advanced AI accelerator currently in mass production, designed for data center-scale workloads. It provides a concrete case of how advanced packaging enables deployable system-level compute under impeded process conditions.

At the chip level, the 910C adopts a dual-die packaging architecture (see Figure 4.1). Two compute dies are linked by high-bandwidth in-package interconnects and share multiple stacks of HBM within a single package. In the taxonomy established in Chapter 2, this design corresponds to Pathway Two, a model based on foundry-OSAT collaboration, using organic substrates and moderate-precision RDLs.

Figure 4.1. Dual-Die Packaging Architecture of Huawei Ascend 910C



Source: Reproduced from Pengfei Zuo et al., Serving Large Language Models on Huawei CloudMatrix384, *arXiv, 2025, Figure 3.*[118]

According to Huawei's published specifications, the 910C delivers approximately 800 TFLOPS of peak compute at FP16 precision, with 128 GB of memory and 3.2 TB/s of memory bandwidth.[119] Industry analyses generally attribute production to SMIC's 7nm-class (N+2) process, while some reporting suggests that TSMC-fabricated components may also be present.[120] Regardless of sourcing, the logic behind the Ascend's design is clear. With limited access to leading-edge nodes, Huawei integrates compute and memory at the packaging level to offset constraints on single-die performance and practical limits on die size.

This design rationale is further extended at the system level through Huawei's CloudMatrix 384 supernode.[121] Designed for large-scale AI training and inference, CloudMatrix integrates 384 Ascend 910C accelerators and 192 Kunpeng CPUs into a highly interconnected architecture.[122] It supports both scale-up through unified bus interconnects and scale-out through high-speed networking, enabling coordinated compute and data flow across nodes. This extends the low-latency, high-bandwidth characteristics of advanced packaging from within the package to the cluster level, helping to alleviate bottlenecks in inter-node communication, memory access, and synchronization. As a result, compute is stable and operationally deployable at data-center scale.

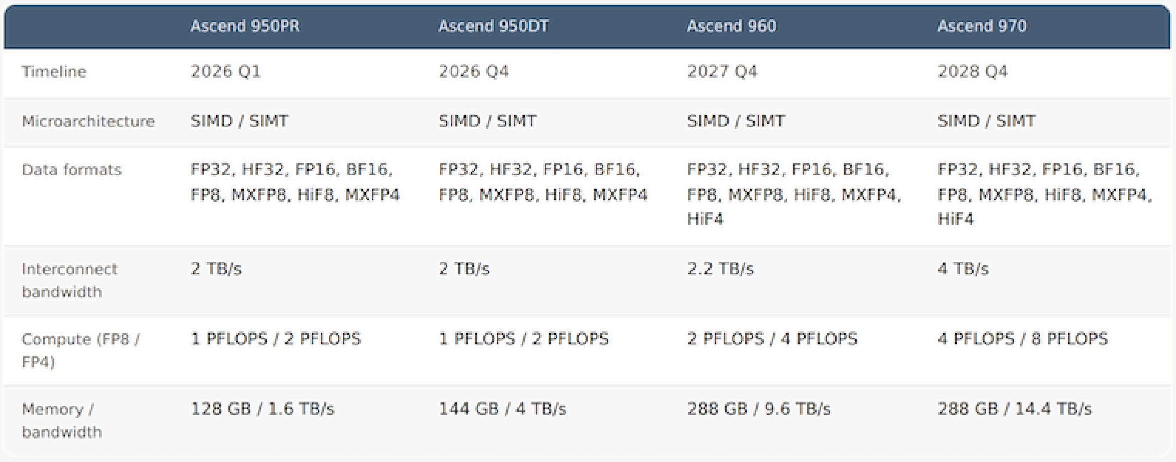
One external data point offers partial validation. A 2025 study by DeepSeek reported that under specific large language model inference configurations, the Ascend 910C achieved roughly 60 percent of NVIDIA H100 inference performance.[123] While these findings are model and configuration specific, they indicate that even without access to leading-edge nodes, a domestically produced accelerator can achieve competitive and deployable inference performance when supported by advanced packaging and system-level integration.

Significantly, the 910C reflects a form of architectural evolution, in which performance is reconfigured through packaging, system design, and integration.[124] However, it remains generally unknown to what extent Huawei's approach can sustain generational improvement under continual process constraints.

4.2 Performance Trajectory: System-Level Scaling Across the Ascend Series

Huawei's roadmap, disclosed at Huawei Connect 2025, reveals some clues about the company's project trajectory under process-constrained conditions (see Table 4.1). The Ascend 950PR, 950DT, 960, and 970 accelerators are scheduled for release between 2026 and 2028.[125] Across these generations, compute density, inter-die interconnect bandwidth, and system-level capabilities advance in parallel, tracing an evolution pathway centered on advanced packaging and system integration.[126] The 950PR debuted in March 2026, marking the first realized step in the roadmap.[127]

Table 4.1. Huawei Ascend AI Accelerator Roadmap and Specifications (2026–2028)



	Ascend 950PR	Ascend 950DT	Ascend 960	Ascend 970
Timeline	2026 Q1	2026 Q4	2027 Q4	2028 Q4
Microarchitecture	SIMD / SIMT	SIMD / SIMT	SIMD / SIMT	SIMD / SIMT
Data formats	FP32, HF32, FP16, BF16, FP8, MXFP8, HiF8, MXFP4	FP32, HF32, FP16, BF16, FP8, MXFP8, HiF8, MXFP4	FP32, HF32, FP16, BF16, FP8, MXFP8, HiF8, MXFP4, HiF4	FP32, HF32, FP16, BF16, FP8, MXFP8, HiF8, MXFP4, HiF4
Interconnect bandwidth	2 TB/s	2 TB/s	2.2 TB/s	4 TB/s
Compute (FP8 / FP4)	1 PFLOPS / 2 PFLOPS	1 PFLOPS / 2 PFLOPS	2 PFLOPS / 4 PFLOPS	4 PFLOPS / 8 PFLOPS
Memory / bandwidth	128 GB / 1.6 TB/s	144 GB / 4 TB/s	288 GB / 9.6 TB/s	288 GB / 14.4 TB/s

Source: Huawei Connect 2025 product roadmap presentation; author's compilation and reconstruction.[128]

Within a single generation, Huawei uses packaging and memory configuration to differentiate system capabilities. The 950PR and 950DT share a similar peak compute tier at FP8, both reaching approximately 1 PFLOPS. Memory bandwidth, however, diverges sharply, from roughly 1.6 TB/s for the 950PR to approximately 4 TB/s for the 950DT. This divergence maps onto workload specialization. The 950PR is configured to favor the compute-intensive prefill stage of inference workloads, while the 950DT is better suited to decode-phase and long-sequence workloads, where higher bandwidth and memory capacity are critical.[129] The design reflects a deliberate strategy to address AI workload bottlenecks through memory subsystem and interconnect configuration.

The Ascend 960 and 970 continue this trajectory. The 960 pushes FP8 compute to approximately 2 PFLOPS and memory bandwidth to 9.6 TB/s, paired with nearly 300 GB of memory capacity. The 970 further amplifies the pattern, with FP8 compute at roughly 4 PFLOPS and memory bandwidth at approximately 14 TB/s. At the engineering level, both the 960 and the 970 reach performance levels sufficient to support large-scale AI model training and inference workloads.

To compare generational progression consistently, this analysis uses Total Processing

Performance (TPP), defined by BIS under ECCN 3A090, as the primary compute metric.[130] Memory bandwidth serves as a complementary indicator.[131] TPP measures the maximum theoretical compute capacity of an IC under conditions most favorable to the chip's stated capabilities. Memory bandwidth reflects the rate at which data can be supplied to compute units, a key determinant of performance in AI workloads. Together, these two axes provide a basis for assessing system-level performance across generations (see Figure 4.2).

Figure 4.2. Huawei Ascend AI Accelerators: Performance Trajectory Across TPP and Memory Bandwidth

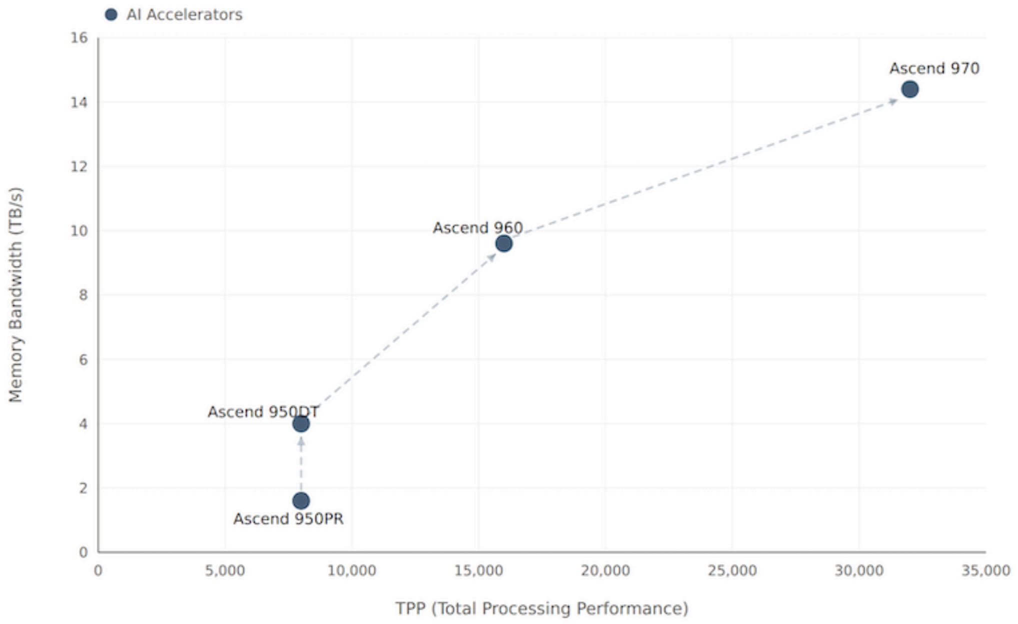


Figure note:

- **a.** Total Processing Performance (TPP) is calculated in accordance with the methodology defined by the U.S. Bureau of Industry and Security (BIS) under ECCN 3A090 Technical Note 2, which specifies the technical scope of the controlled item.[133] TPP measures the maximum theoretical compute capacity of an integrated circuit (IC) under conditions most favorable to the chip's capabilities, with peak performance weighted by the highest supported precision and aggregated across compute units.
- **b.** Memory bandwidth values are drawn from publicly disclosed product specifications and reflect the theoretical maximum data throughput between the chip and its external memory subsystem. For data center–class AI accelerators, this bandwidth is typically provided by HBM architectures and constitutes a key constraint on realized performance.
- **c.** All metrics represent theoretical peak values and do not correspond directly to realized application performance. They are nevertheless indicative of capability boundaries under existing regulatory constraints and provide a basis for comparing system-level design approaches across generations.
- **d.** Specifications for the Ascend 950PR, 950DT, 960, and 970 are based on Huawei's disclosures at Huawei Connect 2025. These figures represent announced performance targets and have not yet been independently validated in production environments.

Source: Huawei Connect 2025 presentations; author's compilation and reconstruction.[132]

Plotted on these axes, the Ascend product sequence from the 950PR through the 970 traces a lower-left to upper-right trajectory, demonstrating gains in both compute capacity and memory bandwidth across successive generations.

Two distinct patterns emerge in this trajectory. Between the 950PR and the 950DT, the shift is nearly vertical. TPP remains constant while memory bandwidth jumps. This reveals that within the same compute tier, packaging and memory configuration can shift where system bottlenecks arise, enabling performance gains without increases in nominal compute. From the 960 to the 970, both compute and memory bandwidth scale upward simultaneously. Performance improvements at this stage are increasingly shaped by multi-die integration, packaging interconnects, and system-level coordination.

Overlaying regulatory and analytical reference points onto this framework clarifies the policy relevance. TPP corresponds to a regulatory threshold defined under U.S. export controls on advanced computing (represented by the red dashed line at TPP = 2,400). This threshold functions as a trigger for additional controls, including performance density requirements. Memory bandwidth serves as an analytical indicator of data transfer capability (represented by the orange dashed line at 1.4 TB/s). Together, they help capture the critical hardware pathways underlying both AI training and large-model inference (see Figure 4.3).

Figure 4.3. Huawei Ascend Processors vs. Export Control Thresholds

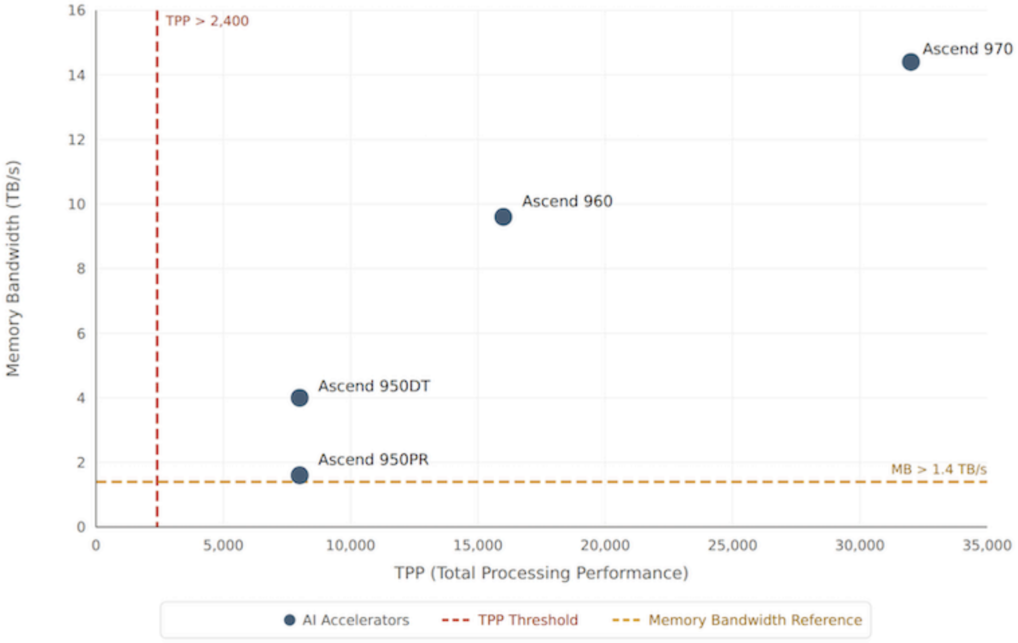


Figure note:

a. TPP is calculated in accordance with the methodology defined by BIS under ECCN 3A090 Technical Note 2. TPP measures the maximum theoretical compute capacity of an IC under conditions most favorable to the chip's capabilities, with peak performance weighted by the highest supported precision and aggregated across compute units.

b. Memory bandwidth values are drawn from publicly disclosed product specifications and reflect the theoretical maximum data throughput between the chip and its external memory subsystem. For data center–class AI accelerators, this bandwidth is typically provided by HBM architectures and constitutes a key constraint on realized performance.

c. All metrics represent theoretical peak values and do not correspond directly to realized application performance. They are nevertheless indicative of capability boundaries under existing regulatory constraints and provide a basis for comparing system-level design approaches across generations.

d. Specifications for the Ascend 950PR, 950DT, 960, and 970 are based on Huawei's disclosures at Huawei Connect 2025. These figures represent announced performance targets and have not yet been independently validated in production environments.

e. The red dashed line, TPP = 2,400, corresponds to the Total Processing Performance threshold defined under BIS ECCN 3A090. This threshold serves as a baseline for triggering additional regulatory conditions, including performance density controls.

f. The orange dashed line, Memory Bandwidth = 1.4 TB/s, is an analytical reference rather than a formally defined regulatory threshold. It is used to approximate performance regimes commonly associated with HBM-integrated, data center–class AI accelerators.

Source: Huawei Connect 2025 presentations; author's compilation and reconstruction.[134]

On theoretical specifications alone, every Ascend product in the planned sequence exceeds both the TPP threshold and the memory bandwidth reference. These specifications are publicly disclosed rather than verified production data, and mass-production capability, performance density, yield, and supply stability remain unverified. These figures should be read as strategic signals about Huawei's intended direction, which indicate system-level optimization driven by packaging and integration, enabling workloads that previously required leading-edge process nodes. Export controls constrain the ceiling of chip-level performance, but system-level compute capability continues to improve, effectively raising the floor of deployable compute.

To place Huawei's trajectory in a broader industry context, Ascend products are compared against NVIDIA's forthcoming AI GPUs across a 2025-2028 window (see Figure 4.4). These NVIDIA GPUs are the performance frontier in data center AI computing. Within this window, 2025 represents the latest mass-produced generation, while 2026–2028 corresponds to publicly disclosed roadmaps from both companies. Huawei's Ascend 910C, 950PR, 950DT, 960, and 970 are plotted against NVIDIA's B300 (Blackwell Ultra), R100 (Rubin), and R200 (Rubin Ultra) on a comparable accelerator-level basis, using TPP and memory bandwidth as common axes.

Figure 4.4. AI Accelerator Performance Trajectories: Huawei Ascend vs. NVIDIA GPUs Across TPP and Memory Bandwidth (2025–2028)

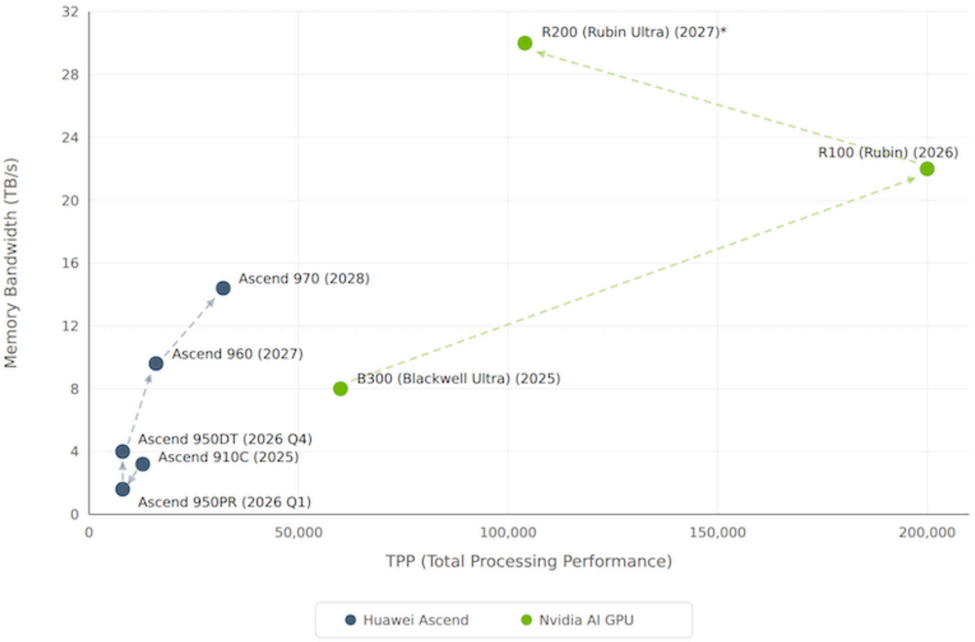


Figure note:

- **a.** TPP is calculated in accordance with the methodology defined by BIS under ECCN 3A090 Technical Note 2. TPP measures the maximum theoretical compute capacity of an IC under conditions most favorable to the chip's capabilities, with peak performance weighted by the highest supported precision and aggregated across compute units.
- **b.** Memory bandwidth values are drawn from publicly disclosed product specifications and reflect the theoretical maximum data throughput between the chip and its external memory subsystem. For data center–class AI accelerators, this bandwidth is typically provided by HBM architectures and constitutes a key constraint on realized performance.
- **c.** All metrics represent theoretical peak values and do not correspond directly to realized application performance. They are nevertheless indicative of capability boundaries under existing regulatory constraints and provide a basis for comparing system-level design approaches across generations.
- **d.** Specifications for the Ascend 950PR, 950DT, 960, and 970 are based on Huawei's disclosures at Huawei Connect 2025. These figures represent announced performance targets and have not yet been independently validated in production environments.
- **e.** Specifications for NVIDIA B300 (Blackwell Ultra) and R100 (Rubin) are based on official technical materials and publicly disclosed product information. For R200 (Rubin Ultra), no official single-GPU specifications have been disclosed. Performance values are estimated based on system-level data from the Rubin Ultra NVL576 platform presented at GTC 2025 and may understate actual per-chip capability. Memory bandwidth is approximated based on expected HBM4e configurations.
- **f.** NVIDIA has announced a subsequent Feynman architecture. However, due to the absence of publicly disclosed specifications, it is not included in this comparison.

Source: Huawei Connect 2025 presentations; NVIDIA technical blog posts, product materials, and keynote presentations; author's compilation and reconstruction.[135]

The Huawei sequence shows a brief performance regression between the 910C and the 950PR, with both TPP and memory bandwidth declining relative to the previous generation. This likely reflects the impact of export control restrictions on access to advanced process nodes and key components.

At comparable generational intervals, NVIDIA's AI GPUs occupy the upper-right of the chart, with substantially higher TPP and memory bandwidth than Huawei's Ascend products. Even as the Ascend series improves across generations, the pace of performance gains remains well below that of NVIDIA's next-generation products. Thus, a clear performance gap persists at the AI accelerator frontier.

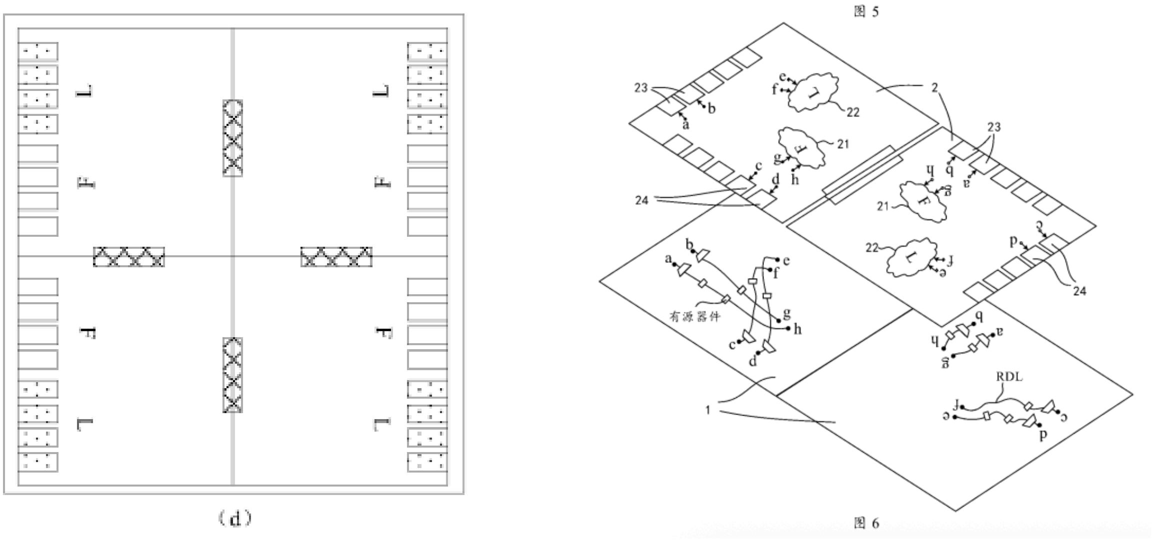
The gap reflects divergent technological foundations across the two trajectories. NVIDIA's performance gains are driven by continued process-node advancement, successive HBM generations, and iterative GPU architecture improvements. Huawei relies instead on advanced packaging, multi-die integration, and high-bandwidth memory to extend system-level compute.

However, the Ascend's trajectory is not static. System-level capability continues to improve across generations, even under export controls. Controls constrain process-node advancement but have not halted the expansion of deployable compute through system-level engineering. Whether this trajectory can be sustained will depend on Huawei's next architectural moves and the ecosystem capable of enabling it.

4.3 Forward Architecture: Quad-Chiplet Integration as the Next Scaling Pathway

A recently disclosed patent for quad-chiplet packaging illustrates a high-density, multi-die integration architecture (see Figure 4.5).[136] This approach reorganizes compute at the system level through packaging, laying the groundwork for future Ascend accelerators.

Figure 4.5. Quad-Chiplet Integration Architecture as a System-Level Scaling Pathway



Source: Reproduced from Huawei patent WO2024222427A1.[137]

The patent centers on integrating four functional dies into a coordinated compute module through advanced packaging structures, including silicon interposers and RDLs. Active components are incorporated within the packaging structure to support high-speed signal transmission. Through high-density silicon interconnects and RDL-based routing, the architecture enables cross-chiplet connectivity and signal optimization.[138] It then establishes a low-latency, high-bandwidth data exchange network within the package, shifting part of the performance burden from the chip level to the packaging and system level. This enables multi-die modules to maintain system stability and energy efficiency under high-density compute deployment.

Technically, this architecture aligns more closely with Pathway One, the foundry-led route optimized for maximum interconnect density. Moreover, the design reflects a twin objective of enhancing system-level performance and deployability while managing cost, manufacturing risk, and supply-chain exposure.

From a performance perspective, the silicon interposer facilitates the reconfiguration of logic blocks, interconnect paths, and I/O interfaces across dies, allowing more flexible signal routing. Active components within the packaging structure take on part of the signal conditioning and interconnect workload, resulting in high-speed inter-die data exchange while maintaining bandwidth and energy efficiency—without full dependence on the most advanced process nodes.[139]

On the manufacturing side, the design integrates RDL with multi-layer embedded structures to increase routing density while reducing package volume and controlling material and process costs. In principle, multi-die architectures of this type can use dies fabricated on higher-yield processes with more stable supply, which are then integrated at the system level through high-density packaging. This approach redistributes manufacturing risk under process-constrained conditions and preserves room for module-level horizontal scaling.[140]

These advantages carry engineering trade-offs, however. High-density multi-die integration demands micron-scale alignment precision, thermal expansion matching between materials, and effective thermal management under high power densities. If these engineering requirements do not mature in step with the architecture, design feasibility may not translate into stable, high-yield volume production.

Industry analysis of the patent suggests that the quad-chiplet architecture may be intended for future Ascend AI accelerators.[141] It also notes parallels with the multi-die integration direction adopted by NVIDIA's next-generation Rubin Ultra platform, which uses TSMC's Chip-on-Wafer-on-Substrate Local (CoWoS-L) technology.[142] CoWoS-L assigns high-bandwidth interconnect functions to Local Silicon Interconnect (LSI) while using RDL for other routing areas, balancing bandwidth, energy efficiency, and integration flexibility.[143]

This parallel is analytically significant. Huawei's quad-chiplet design suggests that its packaging and system-integration approach is aligning with the architectural direction of the global AI accelerator frontier. Under process constraints, Huawei is using back-end integration to close the architectural gap, extending competition beyond process-node advantage into packaging-based system integration.

4.4 Ecosystem Readiness: Capability Alignment Across China's Advanced Packaging Supply Chain

In a competition over AI compute scaling centered on packaging-based integration, no single firm or technology breakthrough can sustain AI compute scaling on its own. The viability of this pathway depends on whether multiple engineering nodes can reach minimum viable capability within a sufficiently narrow time window. The deeper question is whether these capabilities can overlap enough to function as a system. For Huawei to advance its 2.5D/3D and multi-die integration roadmap under process constraints, a domestically sourced supply chain with matched capabilities across key nodes is essential.

A pattern emerges when the capabilities required for the Ascend accelerator line are decomposed into technical modules. Chinese firms are building capacity across 2.5D/3D packaging, high-end substrates, fine-pitch RDL processes, hybrid bonding equipment, and HBM development, forming the early contours of a layered, cross-firm ecosystem (see Table 4.2).

There is an important caveat, though. Huawei's supply-chain relationships are highly opaque and likely to shift under export control pressure. The analysis that follows is based on publicly available information and does not imply confirmed commercial relationships or direct integration into Huawei's production lines.

Table 4.2. Indicative Mapping of Capability Alignment Across China's Advanced Packaging Ecosystem Relevant to Huawei

Company	Capability	Status	Analytical relevance	Evidence
IC Design				
HiSilicon 海思	AI accelerator architecture and chiplet design	Mass production	*Architecture driver shaping multi-die integration strategy*	–
System integrator				
Huawei 華為	AI accelerator platform and full-stack system integration	Mass production	*Core demand anchor defining packaging and system architecture*	–
Foundry / die fabrication				
SMIC 中芯	7nm-class AI accelerator fabrication (N+2 node)	Limited production	*Logic-node constraint driving packaging-based scaling*	Category A
Advanced packaging				
SJ Semiconductor 盛合晶微	2.5D packaging and interposer-based heterogeneous integration	Volume ramp	*Primary packaging execution node for Huawei accelerators*	Category A
Tongfu Microelectronics 通富微电	High-end OSAT and chiplet integration	Mass production	*Large-scale packaging capacity supporting domestic AI chips*	Category A
JCET 长电科技	Heterogeneous integration platforms	Mass production	*Strategic OSAT capacity buffering domestic packaging supply*	Category B
HT-Tech 华天科技	Advanced OSAT, including 2.5D integration and fan-out packaging	Volume ramp	*Secondary domestic OSAT capacity for advanced packaging diversification*	Category A
Substrate & high-density interconnect				
Fastprint 兴森科技	HPC-grade substrate manufacturing	Qualification	*Emerging domestic substitute for high-performance substrates*	Category A
Shennan Circuits 深南电路	High-density ABF and FC-BGA substrates	Volume ramp	*HPC substrate foundation for advanced accelerator packaging*	Category A
Process & equipment enablers				
AMIES 芯上微装	Back-end lithography for RDL patterning	Volume ramp	*Enables fine-pitch RDL for high-density chiplet interconnect*	Category A
Piotech Jianke 拓荆键科	Deposition tools for hybrid bonding and 3DIC processes	Pilot / qualification	*Enables vertical interconnect development for chiplet scaling*	Category B
ACM Research (Shanghai) 盛美半导体	Wet cleaning, electroplating, and wafer-level advanced packaging tools	Mass production	*Supports wafer-level packaging process integration*	Category B
Hwatsing 华海清科	CMP equipment for advanced nodes and packaging	Mass production	*Planarization tools enabling wafer-level packaging processes*	Category B
Materials				
POME 波米科技	Low-dielectric PI materials for RDL and advanced packaging	Qualification	*Localization attempt for dielectric materials bottleneck*	Category A
Anji Microelectronics 安集微电子	CMP slurry for wafer-level and packaging processes	Mass production	*Domestic supplier of CMP consumables supporting wafer-level packaging processes*	Category B
ASEM 艾森股份	Electroplating chemicals for interconnect and advanced packaging metallization processes	Limited production	*Domestic supplier of plating chemicals supporting packaging interconnect processes*	Category A
HHCK 华海诚科	Epoxy molding compounds and advanced packaging encapsulation materials	Mass production	*Supports structural integrity and reliability in high-density multi-die integration*	Category A
Memory integration				
CXMT 长鑫存储	HBM-class memory development and TSV-based DRAM integration	R&D / prototyping	*Memory bandwidth bottleneck constraining AI accelerator scaling*	Category A

Status: Mass production Volume ramp Limited production Qualification R&D / prototyping

Evidence: Category A Category B

Table note:

a. **Scope of mapping.** This list is not intended to be exhaustive, but identifies representative capability nodes across key technical layers required for advanced packaging of AI accelerators. Inclusion reflects publicly reported technological capabilities or analytically inferred alignment within China's advanced packaging supply chain relevant to AI accelerator integration. It does not imply confirmed commercial supply relationships, contractual engagement, or direct integration into Huawei production lines.

b. **Industrialization status.** Industrialization status reflects deployment relevance for advanced packaging in AI accelerator systems, rather than overall company-level production capacity. Classifications are defined as follows:
   - **Mass production:** Technology has reached stable yield and standardized manufacturing processes, and is integrated into large-scale commercial products or deployed systems.
   - **Limited production:** Technology has entered commercial production but remains constrained by yield, capacity, or deployment scope.
   - **Volume ramp:** Technology has passed key customer qualification and entered early commercial shipments, while production lines and yields are still being optimized.
   - **Qualification / Pilot:** Technology is at the customer qualification or pilot-production stage, with prototype products, pilot lines, or limited low-volume output.
   - **R&D / Prototyping:** Technology remains at the research, prototype, or early demonstration stage without commercial production capability.

c. **Evidence classification.** Evidence classification does not apply to Huawei and HiSilicon, which serve as the system integrator and architecture driver, respectively. Categories are defined as follows:
   - **Category A:** Media-referenced collaboration, industry-reported linkage, or widely cited association with Huawei or HiSilicon.
   - **Category B:** Capability presence within China's advanced packaging ecosystem or technological linkage with leading domestic foundries and integrators.

Source: Author's compilation and analysis based on company disclosures, industry reports, and open-source information.[144][145][146][147][148][149][150][151][152][153][154][155][156][157][158][159]

The ecosystem is beginning to take shape across distinct functional layers. SJ Semiconductor, Tongfu Microelectronics, and JCET are building 2.5D/3D and heterogeneous integration capabilities that provide execution capacity for multi-die integration. Fastprint and Shennan Circuits are expanding ABF substrate and high-density routing capabilities that form the structural foundation for high-speed interconnects. AMIES, Piotech Jianke, and related equipment firms are focused on fine-pitch RDL and hybrid bonding processes that determine the physical feasibility of multi-die integration.

These capability nodes are highly interlocked. Under a 2.5D/3D packaging architecture, multi-die integration requires simultaneous alignment across high-end ABF substrate density, RDL line-width precision, hybrid bonding reliability, and memory stacking conditions. If any single node falls below its required engineering threshold, overall system performance cannot be realized. Therefore, the viability of advanced packaging depends on whether multiple nodes achieve viable performance within the same window.

Production-line expansion and equipment investment across these firms have moved broadly in parallel with Huawei's higher-generation Ascend roadmap. In highly specialized process environments such as 2.5D/3D packaging, hybrid bonding, and high-end substrates, production capabilities cannot be easily transferred or reconfigured. Investment patterns embed strong path dependence. Once multiple nodes reach operational capability within a narrow time window, even if maturity levels remain uneven, the mechanisms through which system-level compute performance is assembled can begin to shift incrementally, without waiting for any single bottleneck to be fully resolved.

Across the ecosystem, a clear maturity gradient is emerging. Chip design and system integration, led by HiSilicon and Huawei's platform architecture, constitute the most mature layer. Advanced packaging and heterogeneous integration are in a phase of rapid expansion and engineering optimization, with multiple OSAT and wafer-level packaging firms progressively building

2.5D/3D and multi-die integration capabilities. High-end ABF substrates, critical packaging materials, and HBM remain the principal bottlenecks, with process maturity and supply stability yet to be fully demonstrated.

Among these, two bottlenecks carry particular weight. HBM sets the upper bound on AI accelerator performance scaling, with CXMT representing China's primary domestic node for HBM development and memory-compute integration. Materials and substrate maturity determine whether advanced packaging capabilities can be reliably sustained in production. Key inputs remain concentrated among a small number of Japanese and European suppliers: ABF substrate materials are predominantly controlled by Ajinomoto, while underfill and advanced packaging resins are supplied primarily by Namics and Henkel. Domestic alternatives are expanding, but their maturity varies significantly across nodes, and the ecosystem's capability gap has yet to fully close.

4.5 Policy Implications: Export Controls Under System-Level Compute Dynamics

Process nodes remain foundational to high-end compute competition, and the physical limits of transistor scaling continue to shape single-chip performance. This chapter's assessment of Huawei's product line and technological trajectory shows that as the sources of compute performance diversify, packaging interconnects, memory bandwidth, and system integration are becoming key levers for reconfiguring deployable compute under process-constrained conditions.

Current export control frameworks remain centered on front-end processes, relying primarily on restrictions over key components, equipment, and performance parameters that extend indirectly to related segments. Accordingly, advanced packaging is not treated as an independent, systematic object of control. Under this framework, critical nodes such as advanced packaging materials, high-density substrates, hybrid bonding equipment, and system-integration capabilities are not comprehensively covered. The capability boundaries originally established through node-level restrictions may consequently be circumvented at the system level through alternative optimization pathways. Even where products remain at the stage of announced specifications or limited production capacity, any relaxation of control thresholds could accelerate the maturation of China's domestic technology pathway through market incentives and learning-curve effects. This would ultimately weaken the long-term effectiveness of existing controls.

Therefore, the focus should no longer solely be about whether access to leading-edge processes has been successfully restricted. It should concern whether current control frameworks adequately cover the mechanisms through which advanced packaging and system integration are increasingly reorganizing and amplifying deployable compute. Specifically, export controls should be designed to raise the engineering integration costs and increase resource friction along China's advanced packaging pathway. This would create uncertainty and structural pressure throughout the development process. The effectiveness of export controls will depend on whether they can move beyond single-node restrictions toward dynamic constraints on the broader capability architecture.

Conclusion and Policy Recommendations

Advanced packaging has upended the longstanding view that front-end processes reign supreme. From a technological pathway perspective, advanced packaging is not merely a manufacturing stage but an impetus for semiconductor innovation. It allows firms to push past physical and economic limitations to produce ICs that achieve greater performance, power, energy efficiency, and interconnect density. This is critical for maintaining an edge in the current AI race. Western firms increasingly rely on TSMC's CoWos platform, which is used in Nvidia's leading GPUs.

Conversely, China has deployed a state-directed industrial policy, a whole-of-nation resource mobilization, and targeted subsidies to build an indigenous advanced packaging capacity, as exemplified by Huawei's Ascend series of AI accelerators. The selection of national champions through competition facilitated by local government investment has further concentrated and accelerated this effort. Advanced packaging has become China's primary vehicle for working around export controls on advanced-node chips.

Indeed, the current policy momentum among the United States and other democratic allies and partners leans heavily toward promotion—onshoring capacity, subsidizing domestic fabs, and rebuilding industrial leverage. Unilateral industrial policy has clear limits, however. The more durable path lies in friend-shoring and a democratic division of labor that integrates the comparative advantages of trusted partners, such as Taiwan, the United States, Japan, and Korea, into a coherent, resilient, "non-red" supply chain.

Yet, protect policies, particularly export controls, remain an indispensable tool in both restraining Beijing's indigenization efforts and maintaining a competitive advantage in the semiconductor industry. Under current front-end fabrication controls, China has been denied access to EUV lithography equipment, advanced-node EDA tools, and high-end GPUs. Therefore, rather than retreating from the use of export controls, countries should strategically reform them to address the loopholes.

Through a detailed analysis of the advanced packaging supply chain, this report identifies critical nodes where China remains highly dependent on foreign suppliers along this alternative pathway. It argues that export controls must be extended beyond front-end fabrication to address these dependencies. Accordingly, this report provides policy recommendations structured around four areas:

(1) **Upstream material controls** targeting concentrated supply nodes

(2) **Technology and process controls** governing key manufacturing capabilities

(3) **Product-level controls** addressing downstream procurement risks

(4) **Anti-circumvention mechanisms** to mitigate diversion through third-country transshipment and end-use misrepresentation

Tighten the Grip Over Chokepoints By Extending Export Controls to the Advanced Packaging Supply Chain

The current export control regime is largely dictated by node-centrism and designed around front-end fabrication, primarily restricting China's access to EUV equipment, advanced EDA tools, and high-end AI chips. These controls have effectively constrained China's progress in advanced logic process nodes.

The January 16, 2025 BIS "Foundry Due Diligence" IFR on advanced computing chips extended additional compliance requirements to front-end foundries and back-end OSAT providers by shifting the burden of proof of products' specifications to foundries and OSATs. This rule aimed to prevent design companies from concealing a chip's end-use or end-user to evade controls as BIS explicitly acknowledges that the back-end packaging and testing stages risk circumvention of controls. It noted that certain entities had diverted and subsequently packaged ICs into products exceeding the performance thresholds of ECCN 3A090, the export control classification number for advanced chips.[160] However, the regime remains anchored to a focus on chip-level specifications. It does not systematically incorporate the upstream materials, manufacturing equipment, and process capabilities that enable advanced packaging.

As this report shows, China's circumvention pathway depends on access to high-end packaging materials and manufacturing capabilities that allow system-level performance gains using chips fabricated at its best-available domestic nodes. The effectiveness of the current regime is increasingly shaped not only by restrictions on frontier chips, but by whether it can constrain the broader packaging ecosystem that enables those chips to be integrated into higher-performing systems. Absent such controls, the regime will continue to exhibit a structural gap.

The following sections recommend specific control measures across materials, equipment and process technologies, and downstream products, supported by anti-circumvention mechanisms.

I. Material-Level Controls

Advanced packaging performance and yield are fundamentally shaped by the quality and supply stability of key upstream materials. This report's supply chain analysis identifies several highly concentrated material nodes at AI and HPC grades where China has not yet achieved meaningful indigenous substitution. These nodes constitute chokepoints that create significant leverage for the United States and its allies and partners.

Ajinomoto Build-up Film (ABF). ABF is the core insulating build-up material for high-end FC-BGA substrates, directly determining substrate line width and spacing, interlayer interconnect integrity, and signal transmission performance. It is crucial for AI/HPC chip packaging. The global ABF supply has long been dominated by Japan's Ajinomoto, which commands over 90 percent market share, resulting in a highly concentrated single-supplier structure. China's efforts at indigenous ABF substitution are nascent, with no demonstrated capacity to mass-produce materials meeting high-end substrate specifications. This concentration makes ABF a particularly effective chokepoint. Japan's inclusion of high-specification ABF in its export control or licensing regime could materially constrain China's ability to scale high-end substrate manufacturing, without requiring complex multilateral coordination.

High-End Bismaleimide Triazine Resin (BT Resin). BT resin is another core substrate base material, widely used in FC-BGA and memory packaging. Supply of high-end BT resin is similarly concentrated among Japanese manufacturers, with Mitsubishi Gas Chemical as the primary supplier. Despite ongoing domestic development efforts, China remains highly dependent on Japanese imports for high-specification grades suitable for high-layer-count, fine-line-width substrates. As with ABF film, this concentration makes BT resin a viable target for tightening controls.

High-End Glass Fabric. As advanced packaging for AI applications places greater demands on high-frequency signal transmission, conventional E-Glass fabrics have become increasingly insufficient. Specialty glass fabrics with low dielectric constant and low loss—such as Nitto Boseki's T-Glass—have emerged as critical inputs for high-end substrates. Supply remains highly concentrated in Japan, and China's progress toward substitution in this material category is limited.

Packaging Chemicals and Bonding Materials. Advanced packaging processes rely on a range of high-end chemicals, including underfill, epoxy mold compound (EMC), and Die-Attach Film (DAF), all of which directly affect packaging yield and reliability. High-end products in these categories are supplied predominantly by Japanese firms, with additional participation from European and U.S. suppliers. While China has achieved partial self-sufficiency in low- and mid-grade packaging chemicals, it remains dependent on imports of high-end products such as fine-pitch underfill and low-warpage EMC.

Controls on these materials should be structured around technical thresholds rather than blanket restrictions. Export licensing should be applied to products meeting or exceeding specification thresholds required for advanced packaging used in AI and HPC applications, including parameters such as dielectric loss for ABF, glass transition temperature and interlayer adhesion for BT resin, and dielectric constant for specialty glass fabric. This tiered approach would minimize disruption to the established packaging markets while selectively restricting China's access to materials critical for advanced packaging capabilities.

Given that supply of these materials is highly concentrated in Japan, coordination should be anchored in U.S.-Japan regulatory alignment, with additional participation from other relevant supplier countries as needed. This can be realized through export control coordination with Japan, which pending legislation such as the MATCH and STRIDE Acts aim to achieve. Such targeted coordination can complement the slower consensus-based processes of broader multilateral dual-use export control regimes such as the Wassenaar Arrangement.

II. Equipment and Process-Level Controls

Beyond materials, the realization of advanced packaging depends on a suite of specific manufacturing equipment and process technologies. With front-end fabrication constrained, China is actively developing these back-end capabilities to enhance system-level performance. To limit China's ability to scale along this pathway, this report recommends establishing explicit technical thresholds governing key equipment and process technologies, restricting access to equipment, technology licenses, and technical expertise.

Hybrid Bonding. Hybrid bonding is the core interconnect technology for next-generation advanced packaging. By replacing conventional solder bump connections with direct copper-to-copper bonding, it enables higher interconnect density, lower power consumption, and shorter signal transmission distances. Production-scale capability remains concentrated at TSMC (for SoIC) and select Japanese and European equipment suppliers. While China has invested in R&D, it continues to lag in yield and process stability. Export controls should therefore target core hybrid bonding equipment, including high-precision wafer alignment bonding tools and surface activation processing equipment, as well as associated process technology IP.

2.5D/3D Heterogeneous Integration and Interposer. Silicon interposers and organic interposers are the core carriers for 2.5D packaging, enabling high-bandwidth, short-distance interconnects between multiple dies (such as GPU die and HBM) within a single package. TSMC's CoWoS architecture is built on a silicon interposer. China has made progress in silicon interposer fabrication, but continues to face bottlenecks in large-area yield control, high-density TSV processing, and wafer-level packaging integration. Therefore, export controls should establish technical thresholds for key interposer fabrication equipment—including TSV etch and fill equipment, and wafer-level RDL lithography equipment—based on parameters such as TSV density, RDL line width and spacing, and interposer size.

High-density Substrate Manufacturing. High-end FC-BGA substrates require fine-line-width etching, high-layer-count lamination, precision drilling, and surface treatment. These multiple precision processes directly determine whether a packaged product can support the I/O density and signal integrity requirements of advanced AI chips. Volume production capability of AI-grade high-end substrates is concentrated in Japan (Ibiden and Shinko), South Korea (Samsung Electro-Mechanics and LG Innotek), and Taiwan (Unimicron and Nan Ya PCB). While Chinese firms are rapidly expanding capacity in low- and mid-grade substrates, they remain constrained in producing high-layer-count (16+ layers) high-end FC-BGA substrates with fine line widths (L/S below 8/8μm) at scale, due to limitations in process precision and yield. Thus, export controls should target key substrate manufacturing equipment—including high-precision exposure tools, laser drilling machines, and precision lamination equipment—as well as limiting the licensing of related process technologies.

Micro-bump and Fine-pitch Interconnects. Advanced packaging relies on micro-bump interconnects between dies, between dies and interposers, and across chiplet-based architectures, enabling higher interconnect density. The finer the bump pitch, the higher the interconnect density. Current mainstream advanced packaging has pushed micro-bump pitch below 40μm and continues to advance further. China's capability in fine-pitch bumping remains behind leading OSAT providers in Taiwan and South Korea. Controls should establish technical thresholds based on bump pitch and target associated equipment, including fine-pitch bump placement equipment, mass reflow, and thermo-compression bonding equipment.

Controls on equipment and process technologies should be grounded in explicit quantitative thresholds—such as TSV density, RDL line width and spacing, micro-bump pitch, and substrate layer count and line width—rather than sweeping designations of "advanced packaging technology," to ensure precision and enforceability.

Unlike material supply, key equipment capabilities are distributed across multiple jurisdictions, including Japan (Disco, Tokyo Electron, and Ushio), the Netherlands (the ASML-affiliated Hermes Microvision and BESI), and the United States (SPTS Technologies (KLA), Veeco). As a result, effective controls will require coordinated implementation across major equipment-supplying countries to ensure comprehensive coverage across the advanced packaging equipment ecosystem. Such coordination is essential to prevent regulatory gaps and maintain the integrity of the control regime.

III. Product-Level Controls

A critical downstream gap remains at the product level. Even where upstream controls on materials, equipment, and process technologies are in place, China's access to finished high-end products—including high-end FC-BGA substrates, AI/HPC modules, and integrated server systems—can still enable system-level performance gains. Closing this gap requires product-level measures targeting advanced packaging outputs defined by technical specifications. The following categories warrant specification-based control thresholds:

Finished High-end FC-BGA Substrates. Export licensing requirements should apply to finished FC-BGA substrates whose layer count, line width and spacing, substrate area, and I/O density meet or exceed specifications required for packaging used in AI and HPC applications. These substrates serve as the primary carrier for AI GPU and HPC chip packaging; their acquisition is tantamount to obtaining a critical component of advanced packaging capability. Rather than relying on moving market definitions, control thresholds should be explicitly benchmarked against the physical substrate specifications required to house AI accelerators already subject to U.S. export controls (e.g., those meeting ECCN 3A090 parameters). These baselines must be updated periodically to track the evolving architectures of restricted high-performance systems**.**

AI/HPC Chip Modules and Integrated Systems. Existing controls already cover AI chips exceeding specified computational performance thresholds, such as provisions related to ECCN 3A090. However, as the Foundry Due Diligence IFR revealed, entities may procure chips that approach (but do not reach) control thresholds, and then integrate them through advanced packaging to elevate system-level performance beyond the control standard. The United States should therefore expand the control baseline from "individual chip specifications" to "system-level performance achieved through packaging integration." This approach addresses a key circumvention pathway by anchoring the system-level threshold to the minimum compute density required to efficiently train and deploy frontier foundation models. Targeting aggregated products that breach this functional threshold via chiplet architectures, 2.5D/3D packaging, or multi-chip module (MCM) integration effectively neutralizes the compensatory value of China's packaging-driven strategy.

High Bandwidth Memory (HBM) and Its Packaged Products. HBM is a critical memory component for AI training and inference, and its production depends on advanced packaging technologies such as TSV stacking and hybrid bonding. HBM supply remains concentrated in South Korea (SK Hynix and Samsung) and the United States (Micron), while China continues to lag in domestic capability. Building upon the December 2024 BIS regulations, the U.S. and its allies must strictly enforce and continuously update comprehensive export restrictions on HBM products across all generations (including legacy HBM2/HBM3 stockpiling attempts) to China. Such controls would significantly constrain China's ability to overcome memory bandwidth constraints in its AI compute architecture.

Product-level controls should adopt a triple-layered framework based on destination, end use, and end user. Exporters and intermediaries should be required to declare the final deployment location, application scenario, and end-user identity, supported by an end-user certification regime. This tripartite framework would establish a basis for controlling the downstream deployment of advanced packaging-enabled systems, with enforcement mechanisms further addressed in the following section on anti-circumvention.

IV. Anti-Circumvention Mechanisms

The effectiveness of the preceding controls ultimately depends on enforcement. Without robust audit and verification mechanisms, restrictions on materials, equipment and process technologies, and products can be undermined through third-country transshipment, end-use misrepresentation, and intermediary networks. As geopolitically-driven semiconductor supply chain relocation accelerates, Southeast Asia has emerged as a major hub for back-end manufacturing and assembly, concentrating the risk of diversion. The Foundry Due Diligence IFR indicates that the U.S. government recognizes circumvention risk in the back-end supply chain. However, the current mechanism relies heavily on firm-level self-reporting and lacks a systematic cross-border audit architecture. Anti-circumvention mechanisms should be constructed along the following four dimensions:

Supplier Disclosure and Due Diligence Obligations. While the EAR technically maintains jurisdiction over subsequent reexports and retransfers, current compliance requirements focus primarily on the initial transaction and often lack a systematic mechanism for reporting visibility beyond the first recipient—creating an enforcement blind spot at the final packaging location, final assembly location, and final system deployment location.[161] BIS should strengthen reporting and authorization requirements for the subsequent retransferring of high-risk compute items, thereby establishing a more rigorous, lifecycle-based monitoring framework for critical commercial supply chains.[162]

Anomalous Order Screening Mechanisms. A transaction-data-based anomaly detection mechanism should be established, with heightened scrutiny for the following situations: order volumes inconsistent with an entity's known production capacity; large orders suddenly placed by newly established companies or companies that have recently undergone ownership restructuring; orders for the same end product split into multiple transactions that individually approach but do not reach the control threshold; and orders destined for third countries with elevated transshipment risk. Such screening mechanisms can be embedded in existing export licensing review processes as a risk assessment tool prior to license issuance.

Third-country Transshipment Verification. For regions receiving relocated supply chain capacity, particularly Southeast Asia, periodic and ad-hoc transshipment verification mechanisms should be established. These would involve spot-check cross-referencing of import sources, production records, and shipping destinations at local packaging facilities, substrate manufacturers, and system assembly plants, in order to identify the diversion of materials and products to China. The execution of this mechanism requires bilateral or minilateral cooperation between exporting countries and recipient countries. Priority should be given to establishing verification cooperation frameworks with the primary recipients of semiconductor back-end manufacturing such as Singapore, Malaysia, Vietnam, and Thailand.

Information Sharing and Review Alignment. The effectiveness of the anti-circumvention mechanisms described above depends on the degree of information sharing among countries.

Therefore, the United States, Japan, South Korea, and Taiwan should form the core of a minilateral information-sharing framework focused on high-risk transactions in the advanced packaging supply chain, while developing parallel cooperation mechanisms with key Southeast Asian recipient and transshipment jurisdictions. Shared information should cover high-risk buyer lists, anomalous transaction patterns, known transshipment routes, and shell company structures. The objective is to reduce opportunities for regulatory arbitrage and ensure consistent enforcement across jurisdictions.

Appendix

Advanced Packaging Supply Chain: Vertical Chokepoint Analysis & U.S. Export Control Gaps

Five-Tier Control Gap Overview:

Tier 1 (Materials): ABF film and BT resin are not subject to export controls, constituting the largest policy gap.[163]

Tier 2 (Components): ABF substrates are not directly export-controlled. China lacks AI/HPC-grade volume production capability, but the logic of “locking down equipment = locking down products” breaks down when the materials tier lacks controls.[164]

Tier 3 (Equipment): December 2024 export controls expanded substantially, but laser drilling machines remain outside direct controls, and PrecisioNext’s Thermo-Compression Bonding (TCB) breakthrough indicates the control window is narrowing.[165]

Tier 4 (Packaging): The foundry tier is subject to export controls, but the OSAT layer is precluded. JCET’s XDFOI™ 2.5D is in stable volume production of 4nm multi-chip products, constituting a core bypass node for export controls.[166]

Tier 5 (Chips): Compute-equivalent thresholds cannot cover the chiplet bypass pathway. Huawei’s Ascend 910C demonstrates that even when individual chips are restricted, competitive products can be assembled through packaging.[167]

Tier 1: Upstream Materials.

Supply Chain Node	Leading Supplier	China's Current Technical Status	U.S. EAR Coverage Status	Policy Implications
ABF Build-up Film — Core dielectric layer for FC-BGA substrates.	**Japan:** Ajinomoto Fine-Techno — near-monopoly, >95% market share;[168] Sekisui Chemical.[169] **Taiwan:** WaferChem (晶化科技).[170]	**Currently unable to self-supply.** Guangdong EPSYN (广东伊帕思), Tianhe Jiamo (天和嘉膜), and Shenzhen Niufeisi (深圳市纽菲斯) remain at pilot/sample/small-batch trial production stages.[171] Chinese manufacturers lack volume production records, as the material must satisfy stringent requirements for low-warpage control, low Dk/Df balance, and long-cycle reliability in large-format, high-layer-count FC-BGA substrates.	**Not subject to export controls.**	ABF film is an indispensable functional material for AI chip substrates, and China faces a significant technology gap. **Technology gap × Regulatory gap = Highest-priority node for new export controls.**
BT Resin (Bismaleimide Triazine) — Dielectric layer for memory packaging substrates.	**Japan:** Mitsubishi Gas Chemical (MGC) — original developer and primary supplier; Resonac. **U.S.:** Isola Group, UNION TOOL.[172]	**Partially self-sufficient (mid-to-low-end).** For ultra-low-loss, high-Tg BT specifications required by AI/HPC applications, China remains dependent on MGC materials.	**Not subject to export controls.** Same as ABF film; no direct U.S. controls.	BT resin and ABF film together constitute a dual regulatory gap at the materials tier.
Packaging Chemicals — EMC (Epoxy Molding Compound), Underfill, Die-Attach Film (DAF). Critical chemical materials for packaging yield.	**EMC (top 3 hold ~45% share)[173]:** Sumitomo Bakelite (Japan), Resonac (Japan), Chang Chun Group (長春集團, Taiwan), Scienchem (中科科化, China), Panasonic (Japan), Shin-Etsu Chemical (Japan), Nagase (Japan), Kyocera (Japan), KCC Corporation (Korea), Samsung SDI (Korea), Eternal Materials (長興材料, Taiwan)[174] **Underfill (top 3 hold ~45% share)[175]:** Henkel (Germany), Won Chemical (Korea), NAMICS (Japan), Zymet (U.S.) **DAF (top 4 hold ~60–70% share)[176]:** Resonac (Japan), Henkel (Germany), Nitto Denko (Japan), LINTEC (Japan). **Others:** Hexion (U.S.), Nepes (Korea), Hysolem (Hysol Huawei Electronics' wholly-owned subsidiary, Korea).[177]	**Domestic alternatives remain qualitatively inferior.**[178] HHCK (华海诚科), Hysol Huawei Electronics (衡所华威), Jiangsu Novoray (江苏联瑞新材), Tianjin Kaihua (天津凯华), Jiangsu Zhongpeng New Material (江苏中鹏新材), Beijing Sino-tech Electronic Material (北京科化), among others, maintain product lines. However, as latecomers, Chinese firms lag behind international leaders in volume production know-how and batch-to-batch consistency. HHCK recently acquired Hysol Huawei Electronics, indirectly gaining its wholly-owned Korean subsidiary Hysolem, thereby expanding scale and consolidating resources. HHCK has also successfully entered Huawei's Ascend supply chain and accepted equity investment from Huawei.[179]	**Partially covered.** U.S. vendors fall under EAR; German and Japanese vendors have incomplete coverage (allied coordination gap).	Packaging chemicals play a critical role in die bonding, warpage control, and thermal management for advanced packaging. German, Japanese, and U.S. chemical products serve as essential sources of production stability. Chinese firms are aggressively pursuing domestic substitution. HHCK's Huawei linkage warrants priority monitoring.
Electronic Glass Cloth (E-glass / T-glass) — Reinforcement skeleton for PCB and substrate dielectric layers.	**Japan:** Nittobo — near-monopoly, nearly 90% market share in AI-grade T-glass[180], Asahi Kasei. **Taiwan:** Nan Ya Plastics (南亞塑膠), Taiwan Glass (台玻) — the world's second manufacturer to achieve volume production certification for low-Dk glass cloth.[181] **U.S.:** AGY.	**Standard E-glass:** China is the world's largest fiberglass producer (~70% global share); fully self-sufficient.[182] **Low-Dk / NE-glass:** Henan Guangyuan New Material (河南光远新材), Taishan Fiberglass (泰山玻纤), Grace Fabric (宏和科技), among others, have established low-Dk production lines. China has invested $220M in new D-glass capacity of 15,000 tons.[183] **T-glass (low-CTE):** Only three suppliers worldwide can stably mass-produce IC-substrate-grade low-CTE glass cloth — Nittobo, Taiwan Glass, and Taishan Fiberglass.[184] Taishan Fiberglass, a subsidiary of China National Building Material Group (中国建材集团), is the sole Chinese producer meeting AI server substrate specifications at this materials node.[185] New entrants face extremely high technical barriers, with gaps remaining in quality consistency and capacity.[186]	**Partially covered / Regulatory gap.** Standard E-glass has no EAR controls; high-frequency T-glass specifications are not subject to export controls.	T-glass and low-dielectric specialty glass cloth are functional materials for high-frequency PCBs. China depends on Japanese and U.S. suppliers for high-end specifications.
High-End Copper Foil — HTE (High Temperature Elongation) / RA (Rolled Annealed) / HVLP (Hyper Very Low Profile). Conductor layers for AI server PCBs and high-frequency substrates.	**Japan:** Mitsui Mining & Smelting, Furukawa Electric , JX Advanced Metals — combined ~60% share.[187] Taiwan: Nan Ya Plastics (南亞塑膠), Chang Chun Group (長春集團) Luxembourg: Circuit Foil Korea: ILJIN Materials China: Tongguan Copper Foil(铜冠铜箔), Jiangxi JCC Copper Foil(江铜铜箔), Defu Technology(九江德福), Shandong Jinbao Electronics(山东金宝电子)	**Standard copper foil:** China has ample capacity (Kingboard Copper Foil / 建滔铜箔, Tongling Nonferrous / 铜陵有色, Lingbao Huaxin / 灵宝华鑫, Jiujiang Defu / 九江德福, Shandong Jinbao / 山东金宝, etc.). **HVLP / ultra-thin specifications:** Chinese manufacturers still show a clear technology gap in ultra-low roughness (≤1.0 μm) and ultra-thin (≤12 μm) grades. Three Japanese firms retain dominant market share. Chinese manufacturers (Lingbao Huaxin, Jiujiang Defu, Anhui Tongguang / 安徽铜冠) are on competitor watchlists but have not yet entered the first tier.[188]	**Regulatory gap.** Copper foil (including HTE, VLP, HVLP, and RA high-end specifications) is not on the EAR control list.	High-end HTE / RA copper foil is a critical material for signal integrity in high-frequency PCBs; China has a technology gap in ultra-thin specifications.

Supply Chain Node	Leading Supplier	China's Current Technical Status	U.S. EAR Coverage Status	Policy Implications
CCL (Copper Clad Laminate) — Core base material for PCBs.	**Overall CCL Supplier, top 10 firms hold nearly 70% market share.** **China:** Kingboard (建滔), SYTECH (生益科技). **Taiwan:** EMC (台光電子), Nan Ya Plastics (南亞塑膠), ITEQ (聯茂), TUC (台燿). **Japan:** Panasonic. **Korea:** Doosan Electro-Materials.[189] **Subclass: High-End PCB-Grade CCL / Ultra-High-Frequency M8**[190] **Taiwan:** EMC (台光電子), TUC (台燿), ITEQ (聯茂) **Japan:** Panasonic (Megtron series) **Korea:** Doosan Electro-Materials **Substrate-Grade CCL** (BT, Low-CTE Modified Epoxy; for FC-BGA, HBM packaging substrates)[191] **Japan:** Resonac (41.2%), MGC (22.9%) **Korea:** Doosan Electro-Materials (18.8%)	**Low-to-mid-end CCL:** China has strong indigenous capability. Kingboard and SYTECH rank globally #1 and #2; China accounts for 74.8% of global CCL consumption by value and dominates global high-speed CCL production (~70% share).[192] **Ultra-high-frequency M8 grade:** Chinese firms trail Taiwan, Korean, and Japanese suppliers in technology and certification. U.S. tech giants increasingly rely on Taiwan-Korea-Japan supply chains.[193] **Substrate-grade CCL:** Dominated by Japan and Korea firms.	**Regulatory gap.** CCL is not on the EAR control list.	Driven by demand for high-end GPUs, Taiwan and Korean CCL manufacturers have grown rapidly by entering the NVIDIA supply chain, but China still holds a dominant position at this node overall. That said, no single monopolistic leader has emerged at the CCL node.

⬇ Chokepoint A: Materials → Components — *ABF film and BT resin are not listed under EAR. Packaging chemicals are directly linked to product performance and stability in advanced packaging processes; material sourcing represents a significant Chinese technology gap that remains outside export controls.*

Tier 2: Key Components.

Supply Chain Node	Leading Supplier	China's Current Technical Status (Gap Description & Information Credibility)	U.S. EAR Coverage Status	Policy Implications
ABF Substrate (FC-BGA) — Direct carrier substrate for AI/HPC chips; ≥20 layers, line width <10μm.	**Taiwan:** Unimicron (欣興電子), Nan Ya PCB (南亞電路板). **Japan:** Ibiden, Shinko Electric, Toppan. **Austria:** AT&S. **Korea:** SEMCO. Top 5 firms hold 60% market share.[194]	**Emerging production, but yield and capacity gaps remain in AI ABF substrates.** Chinese firms (Shennan Circuits / 深南电路, Shenzhen Fastprint / 深圳兴森科技, Zhuhai ACCESS / 珠海越亚半导体) appear on global market report competitor lists, but primarily possess BT substrate mass production capability; they remain behind leaders in higher-end ABF substrates.[195] Shennan Circuits announced in 2021 an investment of RMB 6 billion (~$925M) to build ABF substrate production lines, with an annual capacity target of 200 million FC-BGA units — the first Chinese firm to enter this space.[196] China's regional ABF substrate market accounts for ~12% of regional demand, but relies primarily on Taiwanese suppliers.[197] **Dual lock-in:** Upstream dependence on Ajinomoto's exclusive ABF film + laser drilling machine technical barriers; new-entrant investment cycle of 3–5 years.	**Not directly subject to export controls.** ABF substrates themselves have no EAR controls; reliance on indirect coverage through upstream materials and equipment controls. BIS's December 2024 new controls on advanced packaging SME did not extend to substrate products.[198]	ABF substrates are an indispensable intermediate product for AI chips, yet are absent from the control list. The current logic chain ("lock down equipment = lock down products") breaks down when the materials tier has no controls.
Silicon Interposer / RDL Substrate — 2.5D Interposer, TSV process; core structure for heterogeneous integration.	**Taiwan:** TSMC (台積電), UMC (聯電), PSMC (力積電). **U.S.:** Intel. **Korea:** Samsung.[199]	TSV precision, CMP integration, and bridge structure yields remain insufficient. **JCET (长电科技):** XDFOI™ 2.5D pilot line is fully operational and in stable volume production; capable of supplying international clients with 4nm-node multi-chip packaging products.[200] **TFME (通富微电):** Deepening collaboration with AMD to develop CoWoS products.[201] SMIC (中芯国际) can provide mid-tier silicon interposers, but its technical and hardware capabilities remain insufficient to meet the stringent requirements of advanced packaging.[202] IDMs and foundries have an inherent advantage in TSV technology due to front-end process experience; OSAT firms are at a relative disadvantage.[203]	**Indirectly covered.** Dependent on TSMC packaging service controls; silicon interposers themselves have no direct controls. BIS's December 2024 new controls on advanced packaging SME include licensing requirements for packaging companies exporting advanced computing equipment.[204]	Continue monitoring Chinese foundries' capability buildup in TSV/RDL. JCET's XDFOI has reached volume production, indicating substantive progress by Chinese OSATs in 2.5D packaging.

Supply Chain Node	Leading Supplier	China's Current Technical Status (Gap Description & Information Credibility)	U.S. EAR Coverage Status	Policy Implications
HDI PCB — AI server system interconnect boards; 20+ layers, line width <100µm.	**Taiwan:** Zhen Ding Technology (臻鼎科技), Unimicron (欣興電子). **Austria:** AT&S. **Japan:** Meiko. **China:** Victory Giant Technology (胜宏科技), Shennan Circuits (深南电路), WUS Printed Circuit (沪电股份), Suntak Technology (崇达技术), Kinwong Electronic (景旺电子). Taiwan and Chinese manufacturers both hold significant positions at this node.[205]	**China can self-supply, with the technology gap relatively small — and several Chinese firms have advanced to become important suppliers of PCBs for Western leading-edge GPU servers, maintaining deep collaboration with top Western GPU makers.** Victory Giant Technology (胜宏科技) has become a primary HDI PCB supplier for NVIDIA's GB200/GB300 AI server platforms. Within approximately one year, it has advanced from a peripheral position to the top rank in the global AI and HPC PCB market, displacing previously dominant Taiwanese, Japanese, and Korean suppliers.[206] Shennan Circuits, WUS, and Kinwong, among other Chinese manufacturers, are accelerating upgrades toward high-end AI server PCBs.[207] At the industry level, mainland China's PCB sector accounted for ~30.5% of global output in 2023, with HDI boards comprising 27.8% of domestic production.[208]	**Regulatory gap.** HDI PCB is not under EAR; however, China is already self-sufficient.	Unlike ABF film, this node represents a "regulatory gap + China self-sufficiency" scenario. Shenghong Technology has become an NVIDIA Tier-1 supplier, demonstrating strong Chinese competitiveness at this node.

⬇ Chokepoint B: Components → Equipment — *ABF substrates themselves are not on the EAR list. The process-node-centric control assumption that "locking down equipment locks down downstream products" breaks down when upstream materials controls are absent — Chokepoint A and Chokepoint B form a linked vulnerability.*

Tier 3: Manufacturing Equipment.

Supply Chain Node	Leading Supplier	China's Current Technical Status	U.S. EAR Coverage Status	Policy Implications
Thin Film Deposition / Etch Equipment — PVD, CVD, ALD, Etch; core equipment for advanced wafer fabrication.	**U.S.:** Applied Materials, Lam Research, KLA. **Japan:** Tokyo Electron (TEL), Kokusai Electric. **Netherlands:** ASM International. **U.S./UK:** SPTS Technologies (KLA), Veeco.	**Progress exceeding expectations.** NAURA (北方华创): PVD global share rose from 1% to ~10% (2019–2024); ranked 5th globally in equipment sales in 2025.[209] AMEC (中微公司): 5nm etch equipment entered TSMC validation; announced near-completion of development for 20+ types of controlled thin-film equipment.[210] Piotech (拓荆科技): Rapid growth in deposition equipment. Domestic equipment share: 25% in 2024 → 35% in 2025, surpassing the original 30% target.[211]	**Controlled.** BIS' third round of export controls in December 2024 added 24 categories of SME; introduced "node-agnostic" tool controls; added SME Foreign Direct Product Rule (FDPR) with zero *de minimis* threshold (any U.S. component triggers jurisdiction).	Current export controls have been substantially strengthened, but the pace of Chinese domestic substitution poses a fundamental challenge. NAURA has entered the global top 5; AMEC's etch equipment is approaching advanced-node capability. Residual gap: Enforcement loopholes in mature-node DUV equipment controls need reinforcement; China's ability to expand chiplet base capacity using 28nm+ equipment continues to grow.
Laser Drilling Machine — Core equipment for ABF substrate microvia fabrication; CO□ / UV precision laser systems.	**Japan:** Via Mechanics, Mitsubishi Electric, Sumitomo Heavy Industries. **U.S.:** MKS/ESI, Coherent, IPG Photonics. **Germany:** LPKF, Trumpf, Schmoll. **Israel/U.S.:** Orbotech (KLA). **Korea:** EO Technics. **China:** Han's Laser (大族激光), HGLASER (华工雷射, laser subsidiary of Huagong Tech 华工科技), Delphilaser (德龙激光).	**Low-to-mid-end capability exists; high-end gap remains.** Han's Laser is one of the world's largest industrial laser equipment manufacturers and appears on major firm lists in PCB laser drilling market reports.[212] ABF-substrate-grade ultra-high-precision (<50µm) microvia drilling capability still lags, but it is not the case that "no commercial-scale alternative" exists.	**Hardware not directly subject to export controls, but framework has extended.** Laser drilling machine hardware itself remains outside direct EAR coverage. However, in December 2024 controls added ECCN 3D992 for advanced packaging ECAD software. MKS/ESI, as a U.S. company, is directly subject to EAR jurisdiction.	**Key policy gap:** This market features a diversified competitive landscape, and MKS/ESI as a U.S. company can be directly controlled.

Supply Chain Node	Leading Supplier	China's Current Technical Status	U.S. EAR Coverage Status	Policy Implications
Flip-Chip Bonding Equipment — Flip-Chip Bonder, Mass Reflow; precision bonding equipment for advanced packaging.	**Netherlands:** Besi (~24%). **Hong Kong/Germany:** ASMPT/AMICRA (~21–28%). **U.S.:** Kulicke & Soffa (K&S). **Japan:** Shibaura, Toray Engineering, Panasonic. **Korea:** Hanmi Semiconductor. **Germany:** Muehlbauer, SUSS MicroTec. **Austria:** EV Group (EVG). **France:** SET.	**Breakthrough domestic progress emerging.** PrecisioNext (普莱信智能): Self-described as China's only CoWoS-grade TC Bonder developer; Loong series achieves ±1μm placement accuracy; completed first-ever domestic AI chip CoWoS-L packaging test.[213] However, EE Times China notes the Loong series remains unproven in mass production and supports only limited TC-NCF processes.[214]	**Export controls have substantively expanded.** December 2024 BIS added comprehensive China controls on advanced packaging SME. K&S, as a U.S. company, is directly subject to EAR. Applied Materials acquired a 9% stake in Besi in January 2025. ASMPT/Besi have voluntarily restricted shipments to China.	Allied coordination urgently needed — involving not only Netherlands-based Besi, but also Japan (Shibaura), Korea (Hanmi), Germany (SUSS, Muehlbauer), Austria (EVG). PrecisioNext's TCB breakthrough indicates the control window is narrowing. Accelerate inclusion of advanced packaging TCB / Hybrid Bonders on the multilateral control coordination agenda.

⬇ Chokepoint C: Equipment → Packaging Process — *BIS' third round of export controls in December 2024 added advanced packaging SME controls, but laser drilling machine hardware remains outside direct controls, and China's PrecisioNext has completed its first CoWoS-grade TCB packaging test.*

Tier 4: Advanced Packaging Technology.

Supply Chain Node	Leading Supplier	China's Current Technical Status	U.S. EAR Coverage Status	Policy Implications
Foundry Advanced Packaging — CoWoS, SoIC, Foveros, EMIB; AI GPU and HBM integration packaging.	**Taiwan:** TSMC. **U.S.:** Intel. **Korea:** Samsung Foundry.	**China is actively catching up; overall constrained by equipment access.** SJ Semiconductor (盛合晶微): The only Chinese firm with silicon-based 2.5D packaging in volume production (2024); has mastered TSV interposer technology, with chiplet business share rising rapidly.[215] Wuyuan Semiconductor (物元半导体): Focused on hybrid bonding advanced packaging technology; currently in capacity ramp-up phase.[216]	**Strictly Controlled.** TSMC is covered under Taiwan's National Security Act and BIS FDPR. SJ Semiconductor is on the BIS Entity List. However, applying packaging processes using non-U.S. equipment remains a gray area.	**Current controls are effective but limited in scope:** Export controls at this node cover only the top-tier foundry platforms. Chinese advanced packaging firms are also actively investing in 2.5D/3D packaging capacity, creating a potential control breach.
OSAT Advanced Packaging — Fan-Out WLP, SiP, FCBGA; chiplet integration execution layer.	**Taiwan:** ASE (日月光). **U.S.:** Amkor. **China:** JCET (长电科技), TFME (通富微电).[217]	**China is partially capable (core bypass node).** JCET XDFOI™ 2.5D is in stable volume production, delivering 4nm multi-chip packaging products.[218] JCET/TFME both possess 2.5D packaging capabilities. Huawei Ascend 910B/C serves as a representative case.	**Regulatory mismatch.** Jan 2025 rules impose administrative due diligence (transistor verification) on OSATs, but the physical packaging equipment and materials they use remain outside direct EAR controls; JCET / TFME face no direct controls.[219]	**Symptomatic vs. Structural Controls:** Current DD rules target transactions rather than capabilities.; China executes chiplet aggregation through this layer.

⬇ Chokepoint D: Packaging → Final Chips — *While foundry-level advanced packaging faces strict export controls, the OSAT layer remains a critical structural vulnerability. The January 2025 implementation of OSAT due diligence measures targets transactional compliance but leaves the underlying capacity-building mechanisms intact. This regulatory asymmetry—strictly governing the high-end foundry platforms while leaving foundational OSAT equipment and materials largely accessible—allows the "highest-attainable mature dies × chiplet aggregation" pathway to effectively compensate for front-end limitations.*

Tier 5: Final Chip Systems.

Supply Chain Node	Leading Supplier	China's Current Technical Status	U.S. EAR Coverage Status	Policy Implications
AI GPU / Accelerators — NVIDIA H/B series, AMD MI series; AI compute end products.	**U.S.:** NVIDIA, AMD.	Unable to obtain controlled leading-edge models. However, by leveraging unrestricted chiplet packaging pathways, China is successfully deploying compensatory compute capabilities. Huawei's Ascend 910C, achieving approximately 60% of H100 performance, exemplifies this approach.[220]	**Strictly Controlled.** BIS explicitly controls the export of A100/H100 and other high-performance chips based on total processing performance (TPP) and performance density thresholds.	**The limits of node-centric controls:** Compute-equivalent thresholds fail to capture China's workaround pathway. By acquiring uncontrolled materials and equipment, China shifts the technological battlefield to "post-packaging system-level compute" to bypass front-end restrictions.
HBM (High Bandwidth Memory) — HBM2e / HBM3 / HBM3e; essential component for AI accelerators.	**Korea:** SK Hynix, Samsung. **U.S.:** Micron.	**China actively breaking through.** CXMT (长鑫存储) has supplied HBM3 samples to Huawei, targeting volume production by end of 2026. Huawei's Ascend 910C uses legacy-generation HBM from inventory.[221]	**Controlled.** The U.S. brought HBM under export controls (expanded in 2023); December 2024 added HBM-specific controls.[222]	China is aggressively pursuing domestic substitution; CXMT's progress should be monitored.

Table note:

a. **Scope and Methodology.** This table presents a representative—not exhaustive—mapping of the advanced packaging supply chain. Vendor listings at each tier prioritize firms that hold dominant market share, serve as single- or limited-source suppliers for critical nodes, or have documented involvement in China's indigenous substitution efforts. The table does not attempt to catalog every market participant; smaller or emerging vendors may be absent, and the omission of a firm should not be interpreted as an assessment of its strategic insignificance.

b. **Data Currency.** Market share figures, corporate affiliations, and regulatory status reflect publicly available information as of early 2026. The semiconductor packaging landscape is evolving rapidly—particularly with respect to Chinese domestic substitution programs, BIS rulemaking, and allied export control coordination—and readers should verify time-sensitive claims against the most current sources.

c. **Sources.** The analysis draws on industry market reports (Prismark, TrendForce, Mordor Intelligence, DIGITIMES), regulatory filings and rulemaking documents (BIS Interim Final Rules, CRS reports, Covington & Burling legal analyses), company disclosures and press releases, and specialized trade publications. Where claims could not be independently corroborated through multiple sources, they are flagged in the relevant cells or footnotes.

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